MUZAFFARPUR INSTITUTE OF TECHNOLOGY, MUZAFFARPUR

COURSE FILE

OF

DIGITAL ELECTRONICS

(04 1302)

Faculty Name:

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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VISION OF DEPARTMENT

The department is committed for high quality teaching and pursuit of excellence in research. The faculty members of the department are actively involved in research and development in challenging areas of both theory and experiment. We pledge to serve the nation and society by providing skilled and well developed human resource through brilliance in technical education and research.

MISSION OF DEPARTMENT

After successful completion of program, graduates will be able to

PEO1: Work in the infrastructure development projects.

PEO2: Pursue higher studies.

PEO3: Contribute in teaching, research and other developmental activities of electronics & communication engineering and its allied fields.

PEO4: Work in the multicultural and multidisciplinary groups for the sustainable development and growth of electronics and communication engineering projects and profession.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):

After successful completion of program, graduates will be able to

PEO1: Work in the infrastructure development projects.

PEO2: Pursue higher studies.

PEO3: Contribute in teaching, research and other developmental activities of electronics & communication engineering and its allied fields.

PEO4: Work in the multicultural and multidisciplinary groups for the sustainable development and growth of electronics and communication engineering projects and profession.

PROGRAMME OUTCOMES (PO)

PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2	**Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of and need for sustainable development.
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and teamwork:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

COURSE OBJECTIVE AND COURSE OUTCOMES:

Institute / College Name :	MUZAFFARPUR INSTITUTE OF TECHNOLOGY		
Program Name	**B. Tech. Information Technology**		
COURSE CODE	04 1302		
COURSE NAME	**DIGITAL ELECTRONICS**		
Lecture / Tutorial / Practical (per week):	3-1- 2	**Course Credits**	5
Course Coordinator Name	Mr. UMAR FAROOQUE		

Course objective:

The objective of this course is to provide the fundamental concepts associated with the digital logic and circuit design. To introduce the basic concepts and laws involved in the Boolean algebra and logic families and digital circuits. To familiarize with the different number systems, logic gates, and combinational and sequential circuits utilized in the different digital circuits and systems. The course will help in design and analysis of the digital circuit and system.

Course outcomes (CO):

CO1: Became familiar with the digital signal, positive and negative logic, Boolean algebra, logic gates, logical variables, the truth table, number systems, codes, and their conversion from to others.

CO2: Learn the minimization techniques to simply the hardware requirements of digital circuits, implement it, design and apply for real time digital systems.

CO3: Understand the working mechanism and design guidelines of different combinational, sequential circuits and their role in the digital system design.

CO4: Became able to know various types of components-ADC and DAC, memory elements and the timing circuits to generate different waveforms, and also the different logic families involved in the digital system.

MAPPING OF COs AND POs

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	1				1	3	2		3		2
CO2	3	3		2		3	2			3	2	2
CO3	3		3			2				3		2
CO4	3	2				2				3		2

Correlation level: 1- slight (Low) 2- moderate (Medium) 3-substantial (High)

COURSE SYLLABUS:

Topics	Number of Lectures	Weightage (%)
Digital Principle : Analog vs Digital, Number system, Computer Codes, Digital Signals, Waveforms Positive and Negative logic, Logic Gate: basic, universal and others, Truth Table, Logic functions, IC Chips, Timing Diagram, and Electrical analogy.	4	10
Boolean laws and theorems: Logic functions, conversion of logic functions into truth table and vice versa. SOP and POS forms of representation, min terms and max terms, simplification of logic functions by theorems and Karnaugh's map, don't care conditions, design of special purpose computers and related practical problems.	5	13
Analysis and synthesis of combinational logic circuits: Adder and substructures (look-ahead adders), Multiplexers, de multiplexers, Encoders, decoders, code convertors, magnitude comparators, parity generators and checkers**.**	6	17
Integrated circuit logic families : RTL, DTL, TTL, CMOS, IIL/I^2L (Integrated injection logic & emitter coupled logic).	4	10
Sequential Circuits: Sequential circuit blocks and latches, flip flops- race around condition, master slave and edge triggered, SR, JK, D & T Flip Flop, shift registers, counters- synchronous and asynchronous: design of ripple counter.	10	23
Timing circuit : Multivibrators: mono stable and astable timer: LM555.	4	10
ADC and DAC Converters: Use of building blocks in designing larger systems such as digital to analog converters(DAC) weighted resistors and r-2r , analog to digital(ADC)- comparator, counter and succession.	5	12
Memories : Static and dynamic RAMs, ROM, EPROM, and EEPROM.	2	5
	40	

GATE SYLLABUS

Number representations and computer arithmatic (fixed and floating point), boolean algebra, combinational and sequential circuits, minimization.

TIME TABLE

MUZAFFARPUR INSTITUTE OF TECHNOLOGY

B.Tech. 3rd (Third) Semester (2017 Batch) PROVISIONAL TIME TABLE WITH EFFECT FROM 23.07.2018

3RD SEMESTER INFORMATION TECHNOLOGY ROOM NO. 15A								
	9:00 - 10:00	**10:00 - 11:00**	**11:00 - 12:00**	**12:00 – 1: 00**	**1:00 – 2:00**	**2:00-3:00**	**3:00 - 4:00**	**4:00 – 5:00**
MON		DE (IT) (UF) 15A			**R**			
TUES		DE (IT) (UF) 15A			**E**			
WED	DE (IT) (UF) 15A				**C**	DE LAB (UF+SR)		
THUR					**E**			
FRI								
SAT				DE (IT) (T) (UF) 15 A	**S** **S**			
FACULTY NAME : UF : UMAR FAROOQUE								

STUDENT LIST:

SL. NO.	ROLL NO.	NAME	
1	16IT15	BHANU KUMAR RANJAN	
2	16IT07	RISHIKESH BHARDWAJ	
3	16IT30	SUNIL KUMAR	
4	17IT13	RIYA AGRAWAL	
5	17IT16	ANURAG PRAKASH	
6	17IT04	PRATYASHA SHREE	
7	17IT01	ANKIT JHA	
8	17IT03	PREETI	
9	17IT05	SUDHAKAR PRAKASH	
10	17IT12	RISHABH KUMAR	
11	17IT10	NITISH SHRIVASTAVA	
12	17IT08	ALOK KUMAR	
13	17IT07	RAHUL KUMAR SINHA	
14	17IT21	APURVA SINGH	
15	17IT06	ABHISHEK KUMAR	
16	17IT18	RITESH KUMAR	
17	17IT25	ANUPAM SINGH	
18	17IT09	LUV	
19	17IT38	ANURAG GUPTA	
20	17IT31	SHUBHAM KUMAR	
21	17IT32	ARVIND KUMAR	
22	17IT24	SHANTANU KUMAR	
23	17IT19	ESHA NANDINI	
24	17IT35	ABHINAV KUMAR ANAND	
25	17IT22	SHUBHAM KUMAR	
26	17IT28	IFFAT NAAZ	
27	17IT34	VIKASH KUMAR	
28	17IT41	ANKIT KUMAR	
29	17IT36	MD OBAIDULLAH	
30	17IT29	NEESHA BHARTI	
31	17IT20	SURBHI KUMARI	
32	17IT40	SHUBHAM KUMAR	
33	17IT46	AMAN SHRAFF	
34	17IT47	RAKESH KUMAR PRASAD	

35	17IT39	RAHUL KUMAR JHA	
36	17IT27	MALA KUMARI	
37	17IT23	NIVEDITA KUMARI	
38	17IT43	JUHI KUMARI	
39	17IT48	NAVNEET KUMAR	
40	17IT37	MASUM RAJA	
41	17IT44	ABHISHEK KUMAR	
42	17IT42	ANURAG KUMAR SHARMA	
43	17IT45	AKANKSHA ANAND	
44	17IT26	VINEETA	
45	17IT30	KUMAR SHIVAM	

Text Books:

TB1: Digital circuits and design, by S. Salivahanan, and S. Arivazhagan
TB2: Modern digital electronics by R.P Jain, TMH

Reference Books:

RB2: Digital fundamentals by Floyd and Jain, Pearson

COURSE PLAN

Topic No.	Topic	No. of Lecture/ lecture no.	Text book/Reference Book
1.	Analog vs Digital, Digital Signals. Number system, conversion of a number from one number system to other, and Computer Codes, conversion of codes from one code to others.	2	TB1, TB2, RB1
	Waveforms Positive and Negative logic, Logic Gate: basic, universal and others, Truth Table, Logic functions, IC Chips, Timing Diagram, and Electrical analogy.	2	TB1, TB2, RB1
2.	Logic functions, conversion of logic functions into truth table and vice versa. SOP and POS forms of representation, min terms and max terms,	2	TB1, TB2
	Simplification of logic functions by theorems and Karnaugh's map, don't care conditions, design of special purpose computers and	3	TB1, TB2

	related practical problems.		
3.	Adder and substructures (look-ahead adders),	2	TB1, TB2
	Multiplexers, de multiplexers,	1	
	Encoders, decoders, code convertors, magnitude comparators, parity generators and checkers**.**	3	
4.	Sequential circuit blocks and latches, flip flops- race around condition, master slave and edge triggered, SR, JK, D & T Flip Flop.	5	TB1, TB2
	Shift registers	2	
	Counters- Synchronous and asynchronous, design of ripple counter.	3	
5.	ADC and DAC Converters: Use of building blocks in designing larger systems such as digital to analog converters (DAC) weighted resistors and R-2R.	3	TB1
	Analog to digital (ADC) - comparator, counter and succession.	2	
6.	Timing circuit : Multivibrators: mono stable and astable timer: LM555.	4	TB1, TB2
7.	Integrated circuit logic families : RTL, DTL, TTL, CMOS, IIL/I^2L (Integrated injection logic & emitter coupled logic).	4	TB1
8.	Memories : Static and dynamic RAMs, ROM, EPROM, and EEPROM.	2	TB1, TB2
Total Number of Lecture		40	

Question Bank:

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Code : 041302

B.Tech 3rd Semester Examination, 2016

Digital Electronics

Time : 3 hours *Full Marks : 70*

Instructions :

*(i) There are **Nine** Questions in this Paper.*

*(ii) Attempt **Five** questions in all.*

*(iii) **Question No. 1 is Compulsory.***

(iv) The marks are indicated in the right hand margin.

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1. Choose the correct option of the following (any seven): 2×7=14

(a) How many bytes are contained by 32 bits ?

(i) 3

(ii) 4

(iii) 2

(iv) None of the above

(b) If a Hexadecimal number needs to convert to binary. For each hexadecimal digit, there will be how many bits.

(i) 1

(ii) 2

(iii) 4

(iv) 8

(c) The NOR Gate is OR gate followed by

(i) AND gate

(ii) NAND gate

(iii) NOT gate

(iv) None of the above

(d) Digital circuit can be made by the repeated use of

(i) OR gates

(ii) NOT gates

(iii) NAND gate

(iv) None of the above

(e) The Boolean expression: XYZ+YZ+XZ can be reduced to

(i) $\overline{X}$

(ii) Y

(iii) Z

(iv) (X+Y)Z

(f) A full adder circuit may be constructed by using

(i) Two 2-input AND gates and two 3-input OR gates.

(ii) Two half adders and a-2-input AND gates

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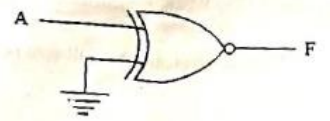
(iii) Two half adders and a 2-input OR gates

(iv) Two 2-input AND gates two 3-input XOR gates

(g) The output of logic gate in the following figure is



(i) 0

(ii) 1

(iii) $\overline{A}$

(iv) A

(h) How many comparators are required to design Parallel Encoded ADC (Flash type ADC) having resolution of 3-bits.

(i) 8

(ii) 7

(iii) 4

(iv) None of the above

(i) Why decoder is used in the digital electronics

(i) To convert coded information into non-coded form

(ii) To convert non-coded information into coded form

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(iii) It is used to separate address bus and data bus

(iv) None of the above

(j) In case of EPROM which one of the following is correct

(i) AND-gate programmable, OR-gate permanently hardwired

(ii) Both AND and OR-gates are programmable

(iii) AND-gate programmable, OUTPUT permanently hardwired but may be taken through Resistor, or tristate gate grammable

(iv) AND-gate permanently hardwired, OR-gate programmable

2. (a) Write down simplified sum of products (SOP) and product of sums (POS) expressions for the Boolean functions: $X=(A+B+C).(A+D).(A+C)$ 6

(b) Implement the full adder by using 1 to 8 demultiplexer. Explain with help of truth table, Boolean equation and block diagram. 8

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(a) What is de-Morgan's theorem ? Solve using this theorem to prove the following:

$$(A+B)\cdot(C+D)=\overline{(A+B)}+\overline{(C+D)}$$ 6

(b) Realize the following function with the help of NAND gates: 8

$$F(A,B,C,D)=\Sigma m(0,1,4,12)+d(2,3,8)$$

4. (a) Write a short notes on any two : 6

(i) Excess-3 code

(ii) Gray code

(iii) 3-bit even parity generator

(iv) 2-bit magnitude comparator

(b) Design a circuit diagram of 4-bit even parity checker using XOR gates. Explain with help of truth table and Boolean equation. 8

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5. (a) Explain the operation of a 2-input CMOS NOR gate. 6

(b) Explain merits and demerits of different logic families. 8

6. (a) Explain the working of D & T Flip-Flops with help of state table, excitation table and block diagram. 6

(b) Design a 4-bit ring counter using D Flip-Flop. 8

7. (a) Differentiate between synchronous and asynchronous counters. 6

(b) Convert J-K Flip-Flop into S-R Flip-Flop. Explain with help of excitation table, characteristic equation and block diagram. 8

8. (a) Explain with the help of a diagram, the principle of operation of R-2R ladder D/A converter. 6

(b) Draw the functional block diagram of timer LM555, and explain how it can be used to obtain a Monostable Multivibrator. 8

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9. (a) Draw the circuit diagram of ROM and explain with sutiable examples. 6

(b) Explain Parallel Encoded ADC (Flash type ADC) with help of block diagram. 8

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2012

DIGITAL ELECTRONICS

Time : 3 hours **akubihar.com** *Full Marks* : 7(

Instructions :

(i) All questions carry equal marks.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Choose the correct answer (any *seven*) :

(a) The decimal equivalent of binary numbe 1101·0011 is

(i) 12·1875

(ii) 13·1875

(iii) 11·1865

(iv) 13·1865

(b) A full adder can be made of

(i) two half adders

(ii) two half adders and a NOR gate

(iii) two half adders and an OR gate

(iv) two half adders and an AND gate

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(c) When two 16-input multiplexers drive a 2-input MUX, what is the result?

(i) 2-input MUX

(ii) 4-input MUX

(iii) 16-input MUX **akubihar.com**

(iv) 32-input MUX

(d) The 'race-around' condition occurs when

(i) $J = 0,\ K = 0$

(ii) $J = 0,\ K = 1$

(iii) $J = 1,\ K = 0$

(iv) $J = 1,\ K = 1$

(e) The maximum possible number of states in a ripple counter with 5 flip-flops is

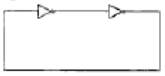
(i) 32

(ii) 15

(iii) 10

(iv) 5

(f) The digital circuit using two inverters shown in the figure will act as



(i) a bistable multivibrator

(ii) an astable multivibrator

(iii) a monostable multivibrator

(iv) an oscillator

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(g) The logic circuit which belongs to non-saturated logic is
  (i) ECL
  (ii) TTL
  (iii) CMOS
  (iv) NMOS

(h) A 12-bit A/D converter has a range of 0–10 V. What is the approximate resolution of the converter?
  (i) 1 mV
  (ii) 2·5 mV
  (iii) 2·5 μV
  (iv) 12 mV

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(i) Which one of the following statements about RAM is not correct?
  (i) RAM stands for random access memory
  (ii) It is also called read/write memory
  (iii) When power supply is switched off, the information in RAM is usually lost
  (iv) The binary contents are entered or stored in the RAM chip during the manufacturing

(j) The minimum number of flip-flop required to construct a mod-75 counter is
  (i) 5
  (ii) 6
  (iii) 7
  (iv) 8

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2. (a) Draw a full-adder circuit and explain its operation.

   (b) Explain the general principle of counter-type A/D converter.

3. (a) State and prove de Morgan's theorem. How is it helpful in minimizing a given Boolean expression?

   (b) Show that
   (i) $\overline{\overline{A}+B}+\overline{\overline{A}+\overline{B}}=A$
   (ii) $(A+B)(B+C)(C+A)=AB+BC+CA$
   (iii) $AB+\overline{B}\,\overline{C}+A\overline{C}=AB+\overline{B}\,\overline{C}$

   (c) Simplify $B+A\overline{B}+AB$.

4. (a) What is *J-K* flip-flop? How can problems associated with *R-S* flip-flop be eliminated with the help of *J-K* flip-flop?

   (b) Design a 3-bit synchronous counter using *J-K* flip-flops.

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5. (a) How do you realise a parity bit checker?

   (b) Describe the operation of the parallel in serial out shift register with neat logic diagram.

6. Design a mod-8 up-down counter.

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7. *(a)* Design a 100 kHz, 60% duty cycle square wave generator using 555 timer.

   (b) A D/A converter has a full-scale analog output of 10 V and accepts six binary bits as inputs. Find the voltage corresponding to each analog step.

8. A digital system has four bits of a 4-bit word *ABCD* as inputs. The output *Y* is equal to 1 when any two adjacent bits are 1, or any three or all four bits are 1.

   (a) Draw the Karnaugh map for *Y*.

   (b) Realise *Y* using 2-input and gates only.

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9. Write short notes on the following :

   (a) EEPROM

   (b) DTL logic

   (c) Race-around condition

   (d) Encoders

* * *

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Code : 041302

B.Tech 3rd Semester Exam., 2015

DIGITAL ELECTRONICS

Time : 3 hours | *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Choose the correct option of the following (any *seven*) : 2×7=14

(a) Universal gate is

(i) AND gate

(ii) OR gate

(iii) NAND gate

(iv) XOR gate

(b) Number of minimum 2-input NAND gates required to make half-adder circuit is

(i) 2

(ii) 3

(iii) 4

(iv) 5

(c) Which one of the following is a sequential circuit?

(i) Mux

(ii) Half-adder

(iii) Demux

(iv) Flip-flop

(d) Which one of the following circuits is a combinational circuit?

(i) Counter

(ii) Register

(iii) Memory

(iv) Mux

(e) Number of flip-flop required to make modulo-6 counter is

(i) 1

(ii) 2

(iii) 3

(iv) 4

(f) Combinational circuit output depends upon

(i) present input

(ii) present output

(iii) previous output

(iv) None of the above

(g) Sequential circuit output depends upon

(i) present input and previous output

(ii) present input and present output

(iii) only present input

(iv) None of the above

(h) For the design of one full-adder circuit, the required number of half-adder is

(i) 1

(ii) 2

(iii) 3

(iv) 4

2. (a) Draw the circuit diagram of full-adder circuit using NAND gates. 6

(b) Draw and explain the circuits of monostable and bistable multivibrators. 8

3. (a) Draw the circuit diagram of 1 : 8 demux and explain. 6

(b) Design priority encoder and explain the circuit with suitable truth table. 8

4. (a) Draw the circuit diagram of 2-input NAND gate using CMOS logic and explain the switching action of the transistors. 6

(b) Explain the differences between TTL and CMOS logic. 8

LIST OF THE EXPERIMENTS

1. Truth table verification of different logic gates- AND, OR, NOT, NAND, NOR, X-OR, and X-NOR.
2. Realization of basic Gates using universal Gates.
3. Design of half and full adder circuits.
4. Design of half and full subtractor circuits.
5. Design of code converters circuits-Binary to Gary code, and Gray to Binary code.
6. Design of magnitude comparator circuits.
7. Study of multiplexer (MUX) & demultiplexer (DEMUX) circuits.
8. Design of shift register.
9. Study of different types of Flip Flops (FFs)-SR-FF, JK-FF, D-FF, and T-FF.
10. Conversion from one Flip Flop (FF) to others.