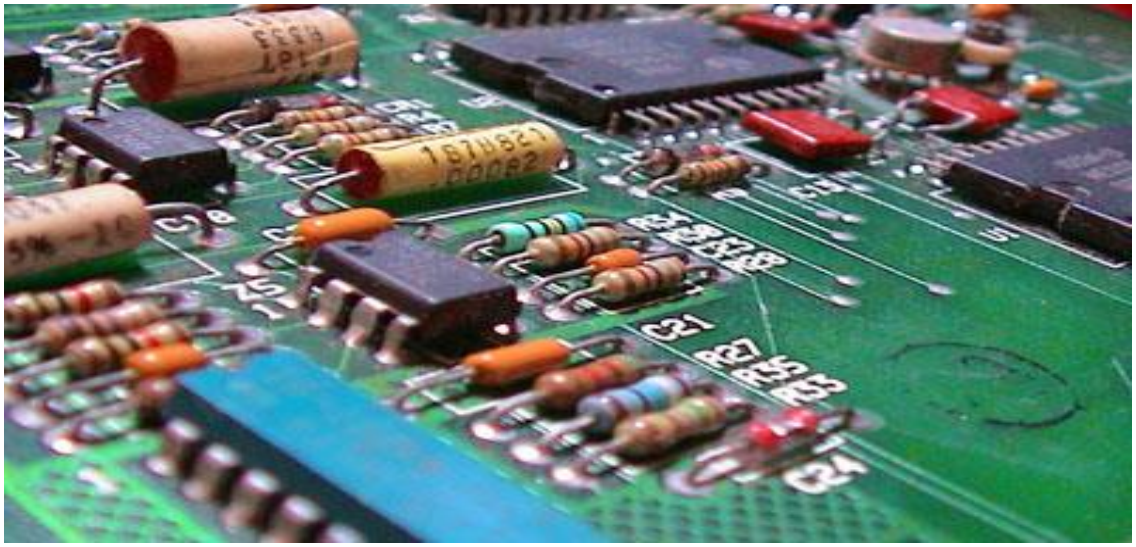
MUZAFFARPUR INSTITUTE OF TECHNOLOGY, Muzaffarpur

COURSE FILE

OF

Digital Electronics

(041402)



Faculty Name:

MR. HARI CHARAN VERMA

ASSISTANT PROFESSOR, DEPARTMENT OF ELECTRICAL ENGINEERING

Content

Govt. of Bihar

MUZAFFARPUR INSTITUTE OF TECHNOLOGY,
MUZAFFARPUR-842003

(Under the Department of Science & Technology Govt. of Bihar, Patna)

VISION STATEMENT OF ELECTRICAL ENGINEERING DEPARTMENT

To produce cutting edge Electrical Engineers, innovators, researchers, and entrepreneurs with high human values to serve society, industry, nation and the world.

MISSION STATEMENT OF ELECTRICAL ENGINEERING DEPARTMENT

M1. To create state-of-the-art facilities for under-graduate, post- graduate and R&D work.

M2. To cater the needs of society with recent technologies, innovative ideas and inculcate ethical responsibilities.

M3. To develop strong collaborative links with premier industries, institutions and the government agencies.

Program Educational Objectives (PEOs) of Electrical Engineering Department:

PEO 1. Students will be able to engage in life-long learning and research including supportive and responsible roles on multi-disciplinary tasks.

PEO 2. Students will acquire, use and develop skills as required for effective professional and societal practices and leadership quality.

PEO 3. Students will be able to create a new dimension of innovation and entrepreneurship.

Program Outcomes (POs) based on Program Educational Objectives (PEOs) of Electrical Engineering Department:

PO 1. Students will be able to apply knowledge of applied mathematics & science in electrical engineering problems.

PO 2. Students will be able to identify, formulate and solve society and industries related problems.

PO 3. Students will be able to apply knowledge to design a system, component or process to meet desired needs within realistic constraints.

PO 4. Students will be able to conduct laboratory experiments and to critically analyze and interpret experimental data.

PO 5. Students will be able to use the recent techniques, skills, and modern tools necessary for engineering practices.

PO 6. Students will be able to understand the impact of engineering problems, solutions in a global and societal context.

PO 7. Students will be able to demonstrate professional and ethical responsibilities.

PO 8. Students will be able to apply leadership quality to work with team in the area of electrical engineering towards the solution of multi-disciplinary tasks.

PO 9. Students will be able to communicate effectively through verbally, technical writing, reports and presentation.

PO 10. Students will be able to develop confidence for self-education and ability to engage in life-long learning.

COURSE OBJECTIVE AND COURSE OUTCOMES:

Institute/college Name	Muzaffarpur Institute of Technology, Muzaffarpur
Program Name	B.E. Electrical (IV semester)
Course Code/course credits	041402 (5)
Course Name	Digital Electronics
Lecture/ Sessional (per week)	3/1
SEE duration	4 hours
Course Coordinator Name	Mr. Hari Charan Verma

Course objective:

To acquire the basic knowledge of digital logic levels and application of knowledge to understand digital electronics circuits. To prepare students to perform the analysis and design of various digital electronic circuits.

Course outcomes (CO):

CO1: Understanding the different number systems used in computerized system and codes used to represent the digits and fundamental of arithmetic operation using each number system and codes.

CO2: Understanding the minimization of logic expression and designing combinational and sequential digital circuits.

CO3: The ability to identify and prevent various hazards and timing problems in a digital design

CO4: Ability to identify basic requirements for a design application and propose a cost-effective solution. To develop skill to build and troubleshoot digital circuits.

CO5: Enabling students to take up application specific sequential circuit to specify the finite state machine and designing the logic circuit.

MAPPING OF COs AND POs

Sr. No.	Course Outcome	PO
1.	**CO1**: Understanding the different number systems used in computerized system and codes used to represent the digits and fundamental of arithmetic operation using each number system and codes.	PO1, PO2, PO3, PO5, PO9, PO10
2.	**CO2**: Understanding the minimization of logic expression and designing combinational and sequential digital circuits.	PO1, PO5, PO6, PO7
3.	**CO3**: The ability to identify and prevent various hazards and	PO1, PO4, PO8

	timing problems in a digital design.	
4.	**CO4**: Ability to identify basic requirements for a design application and propose a cost-effective solution. To develop skill to build and troubleshoot digital circuits.	PO1, PO2, PO9, PO10
5.	**CO5:** Enabling students to take up application specific sequential circuit to specify the finite state machine and designing the logic circuit.	PO1, PO3, PO4, PO5, PO7,PO9,PO10

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10
CO1	√	√	√	-	√	-	-	-	√	√
CO2	√	-	-	-	√	√	√	-	-	-
CO3	√	-	-	√	-	-	-	√	-	-
CO4	√	-	√	√	√	-	√	-	√	√

Course Syllabus:

UNIT-I

Digital Principle: Analog vs Digital, Number system, Computer Codes, Digital Signals, Waveforms Positive and Negative logic, Logic Gate: basic, universal and others, Truth Table, Logic functions, IC Chips, Timing Diagram, Electrical analogy.

Boolean laws and theorems: Logic functions, conversion of logic functions into truth table and vice versa. SOP and POS forms of representation, min terms and max terms, simplification of logic functions by theorems and Karnaugh's map, don't care conditions, design of special purpose computers and related practical problems.

UNIT-II

Analysis and synthesis of combinational logic circuits: Adder and substructures (look ahead adders), Multiplexers, de multiplexers, Encoders, decoders, code convertors, magnitude comparators, parity generators and checkers.

Integrated circuit logic families: RTL, DTL, TTL, CMOS, IIL/I2L (integrated injection logic & emitter coupled logic).

UNIT-III

Sequential circuit blocks and latches, flip flops-race around condition, master slave and edge triggered, SR, JK, D & T Flip Flop, shift registers, counters-synchronous and asynchronous: design of ripple counter.
Timing circuit: multi vibrators, mono stable and astable timer: LM555.

UNIT-IV

Use of building blocks in designing larger systems such as digital to analog converters (DAC) weighted resistors and r-2-r, analog to digital(ADC)-comparator, counter and succession.

Memories: static and dynamic RAMs, ROM, EPROM, EEPROM.

Books:

- **Digital fundamentals by Floyd And Jain, Pearson.**
- **Modern digital electronics by R.P Jain, TMH**
- **Digital systems -Principles and Applications by Tocci, Widmar and Jain, Pearson**

GATE Syllabus of Digital Electronics:

Section: Analog and Digital Electronics

Characteristics of diodes, BJT, MOSFET; Simple diode circuits: clipping, clamping, rectifiers; Amplifiers: Biasing, Equivalent circuit and Frequency response; Oscillators and Feedback amplifiers; Operational amplifiers: Characteristics and applications; Simple active filters, VCOs and Timers, **Combinational and Sequential logic circuits, Multiplexer, Demultiplexer, Schmitt trigger, Sample and hold circuits, A/D and D/A converters,** 8085Microprocessor: Architecture, Programming and Interfacing.

MUZAFFARPUR INSTITUTE OF TECHNOLOGY

B.Tech. 4th (Fourth) Semester (2016 Batch)

DAY	I (10-10.50AM)	II (10.50-11.40AM)	III (11.40-12.30PM)	IV (12.30-01.20PM)		V (01.50-1.40PM)	VI (2.40-3.30PM)	VII (3.30-4.20PM)
MON	Dig Elec (HCV)33	O.B.I.P (SK)33	I.E&A (IH) 33	PS 1(YNS) 33		NMCT (SKJ)33		
TUE					B	PS 1(YNS) 33	PS 1-T(YNS) 33	NMCT (SKJ)33
WED	I.E & A (I H) 33	Dig Elec (HCV)33			R	……..NMCT Lab(SKJ)……		
THU	Elect Mc 2(RKM) 33	O.B.I.P (SK)33	NMCT (SKJ)33	I.E & A (I H) 33	E	PS 1(YNS) 33	Elect Mc 2(RKM) 33	
FRI	Dig Elec (HCV)33	Dig Elec-T(HCV) 33	O.B.I.P (SK)33	Elect Mc 2(RKM) 33	A	…….. Elect Mc 2 Lab (RKM)/ Dig Elec Lab(HCV+MS)…….		
SAT	Dig Elec (HCV)33	….. Elect Mc 2 Lab (RKM)/ Dig Elec Lab(HCV+MS)…….			K			

HCV-Hari Charan Verma, SK-santosh Kumar, RKM- Roushan Kumar Mishra, IH- Irfan Haider, YNS- Yagyanand Sharma

Asst.Prof.-in-charge (TT) Prof.-in-charge (TT) Principal

STUDENT LIST:

S.NO.	*Roll No*	*Name*
1	16EE01	NANDAN KUMAR
2	16EE02	ANJALI KUMARI
3	16EE03	KAUSTUBHA
4	16EE04	RISHABH KUMAR
5	16EE05	AMRITA KUMARI
6	16EE06	SUMIT KUMAR
7	16EE07	RITESH RAJ
8	16EE08	VIPUL MISHRA
9	16EE09	SAMEER KUMAR
10	16EE10	MD SAIFULLAH SADIQUE
11	16EE11	PREETI KUMARI
12	16EE12	KULDEEP THAKUR
13	16EE13	SHANTANU KUMAR SINGH
14	16EE14	SEEMA KUMARI
15	16EE15	PRIYAM KUMARI
16	16EE16	VANDANA BIHARI
17	16EE17	RAJNANDANI
18	16EE18	SANJAY KUMAR YADAV
19	16EE19	PRAVEEN DIVAKAR
20	16EE20	AMIT KUMAR PANDIT
21	16EE21	CHANDAN KUMAR THAKUR
22	16EE22	ALOK KUMAR
23	16EE23	DEVENDRA KUMAR
24	16EE24	ARVIND KUMAR
25	16EE25	AMITESH KUMAR
26	16EE26	VIVEK KUMAR
27	16EE27	VIKASH KUMAR RAY
28	16EE28	ROHIT KUMAR

29	16EE29	OM PRAKASH KUMAR
30	16EE30	RAVI KUMAR
31	16EE31	SANDEEP KUMAR
32	16EE32	DEO ALOK
33	16EE33	BAJRANGI KUMAR
34	16EE34	MANOJ KUMAR SONI
35	16EE35	SANJEEV KUMAR
36	16EE36	NEERAJ KUMAR
37	16EE37	SATYAM KUMAR
38	16EE38	PRASHANT GAURAV
39	16EE39	NITISH KUMAR RAJAK
40	16EE40	UJJAWAL KUMAR
41	16EE41	PRABHAT KUMAR
42	16EE42	MD HASIM JILANI
43	16EE43	SHIV CHARAN KUMAR
44	16EE44	ANISH BHARTI
45	16EE45	RAHUL KUMAR
46	16EE46	RAJEEV RANJAN PRASAD
47	16EE47	SHUBHAM KUMAR
48	16EE48	TAHIR QAMAR
49	16EE49	PRASHANT KUMAR
50	16EE50	NAMAN KUMAR
51	16EE51	KESHAV CHANDRA
52	16EE52	SWETA BHARTI
53	16EE53	PRATIK ANAND
54	16EE54	SHAGUFTA ANJUM
55	16EE55	GOLDEN KUMAR
56	16EE56	MURLI MANOHAR
57	16EE57	ARPIT ANAND
58	16EE58	AKSHAT RAJ
59	16EE59	ANJAN KUMAR
60	16EE60	SUMAN KUMAR BHARTIYA

62	16EE61	SAKET
63	16EE62	RISHABH KUMAR
64	16EE63	SUMAN KUMAR
65	16EE64	SUNITA KUMARI
66	16EE65	NISHANT RAJ
67	16EE66	VIPIN SINGH
68	16EE67	ANKIT RAJ
69	16EE68	GUNJAN KUMAR
70	16EE69	PRATAP CHANDRA CHOUDHARY
71	17(LE)EE01	VIVEK KUMAR
72	17(LE)EE02	RITIK KUMAR
73	17(LE)EE03	ANAND RANJAN
74	17(LE)EE04	ABHISHEK KUMAR
75	17(LE)EE05	POONAM KUMARI
76	17(LE)EE06	SAURABH KUMAR JHA
77	17(LE)EE07	PARMANAND KUMAR
78	17(LE)EE08	ROHAN RAJ
79	17(LE)EE09	ANAND KUMAR
80	17(LE)EE10	MANISH

Course Plan:

Text Books:

TB1: Mano, Morris. "Digital logic." *Computer Design. Englewood Cliffs Prentice-Hall* (1979).

TB2: Kumar, A. Anand. *Fundamentals Of Digital Circuits 2Nd Ed*. PHI Learning Pvt. Ltd., 2009.

TB3: Digital systems - Principles and Applications by Tocci, Widmar and Jain, Pearson

TB4: Digital fundamentals by Floyd And Jain, Pearson

Reference Books:

RB1: Fundamentals of VHDL design by Stephen Brown and Zovenkeo Vraseseic, TMH

RB2: Introduction To Logic Design With Cd Rom by Alan B Marcovity, TMH,

RB3. Fundamentals Of Digital Logic With Verilog Design by Stephen Brown, TMH

RB4. Modern digital electronics by R.P Jain, TMH

Other readings and relevant websites

S.No.	**Link of Journals, Magazines, websites and Research Papers**
1.	http://nptel.ac.in/courses/117106086/1
2.	http://nptel.ac.in/courses/117106114/
3.	http://www.engpaper.com/electronics.htm
4.	http://www.newelectronics.co.uk/digital-magazine/
5.	http://journalspub.com/journalspub/AllEditorsJournalwise.aspx?jid=25&jname=International+Journal+of+Digital+Electronics

COURSE PLAN

Lecture Number	Topics	**Web Links for video lectures**	**Text Book / Reference Book**	**Page numbers of Text Book(s)**
1-4	Digital Principle		TB4, TB1, RB4	2-130(TB4)
	Analog vs Digital, Number system, Computer Codes, Digital Signals, Waveforms Positive and Negative logic, Logic Gate: basic, universal and others, Truth Table, Logic functions, IC Chips, Timing Diagram, and Electrical analogy.	https://www.youtube.com/watch?v=CeD2L6KbtVM		

5-9	**Boolean laws and theorems**		TB1, TB4,TB2	132-220(TB4)
	Logic functions, conversion of logic functions into truth table and vice versa. SOP and POS forms of representation, min terms and max terms, simplification of logic functions by theorems and Karnaugh's map, don't care conditions, design of special purpose computers and related practical problems.	https://www.youtube.com/watch?v=WfA4zlARZ7k		
9-15	**Analysis and synthesis of combinational logic circuits**		TB4, TB2, RB4	222-290(TB4)
	Adder and substructures (look ahead adders), Multiplexers, de multiplexers, Encoders, decoders, code convertors, magnitude comparators, parity generators and	https://www.youtube.com/watch?v=uv_RJ1Pv71s		
16-19	**Integrated circuit logic families**		TB4, RB1	578-605(TB4)
	RTL, DTL, TTL, CMOS, IIL/I2L (integrated injection logic & emitter coupled logic).	https://www.youtube.com/watch?v=iqENkJnJiwc		
20-29	**Sequential circuit blocks and latches**		TB4, TB3, RB3	292-419(TB4)
	flip flops- race around condition, master slave and edge triggered, SR, JK, D & T Flip Flop, shift registers, counters- synchronous and asynchronous: design of ripple counter.	https://www.youtube.com/watch?v=ibQBb5yEDlQ		
30-31	**Timing circuit**		TB1, RB2	
	multi vibrators, mono stable and astable timer: LM555	https://www.youtube.com/watch?v=tpVUl_y0EyQ		
32-33	**Use of building blocks**		TB1, RB4	
	designing larger systems such as digital to analog converters(DAC) weighted resistors and r-2r , analog to digital(ADC)- comparator, counter and succession.	https://www.youtube.com/watch?v=Y2OPnrgb0pY		
34-35	**Memories**		TB4, TB2, RB4	422-472(TB4)
	static and dynamic RAMs, ROM, EPROM, and EEPROM.	https://www.youtube.com/watch?v=GnOTczdBWh8		

Lab Plan

S. No.	Experiment Detail
1	**To study basic gates (AND, OR, NOT, NAND, NOR, EX-OR) and verify their truth tables.**
2	To design and verify operation of half adder and full adder.
3	To design and verify operation of half subtractor and full subtractor.
4	To design and verify BCD to 7 segment Decoder.
5	To design and verify shift register.
6	To design and verify Counter logic.

DETAILS OF ASSIGNMENTS:

S.No.	Assignment	Topic No.
1	Assignment 1	1
2	Assignment 2	2

DETAILS OF TUTORIAL:

S.No.	Tutorial	Topic No.
1	Tutorial 1	1
2	Tutorial 2	2
3	Tutorial 3	2
4	Tutorial 4	3
5	Tutorial 5	3

Digital Electronics (EE-041402)

Tutorial 1

1. Write down simplified sum of products (SOP) and product of sums (POS) expressions for the Boolean expression: X= $(A+B+C).(A+D).(A+C)$

2. Implement the full adder by using 1 to 8 demultiplexer. Explain with help of truth table. Boolean equation and block Diagram.

3. Write a short notes on : (a) Excess-3 code (b) Gray code (c) 3-bit even parity generator (d) 2-bit magnitude comparator.

4. (a) What is de-Morgan's theorem. Solve using this theorem to prove the following:

$$(A+B).(C+D)=\overline{(A+B)+(C+D)}$$

(b) Realize the following function with the help of NAND gates:

$$F(A,B.C,D)=\sum m(0,1,4,12)+d(2,3,8)$$

5. (a) Design a full adder using only NAND gate.

(b) Design a 8 to 1 line multiplexer using 4 to 1 line multiplexer.

Digital Electronics (EE-041402)

Tutorial 2

1. (a) Make a K-map for the function : $F=A\overline{B}+AC+A\overline{D}+AB+ABC$

(b) Express F, in standard SOP and POS form.

(c) Minimize F and realize the minimal expression using NOR gate only.

2. Prove the following algebraically:

(i) $(A+B)(A+\overline{B})=A\oplus B$

(ii) $(A+B)(A+\overline{B})(\overline{A}+B)=AB$

3. (a) Draw a full-adder circuit and explain its operation.

(b) how do you realize a parity bit checker.

(c) simplify $B+A\overline{B}+AB$

4. Show that :

(i) $\overline{\overline{A}+B}+\overline{\overline{A}+\overline{B}}=A$

(ii) $(A+B)(B+C)(C+A)=AB+BC+CA$

(iii) $AB+\overline{B}\overline{C}+A\overline{C}=AB+\overline{B}\overline{C}$

5. Write short notes on following:

(a)Decodes (b) Encodes (c) Multiplexer (d) De-multiplexer

Digital Electronics (EE-041402)
Tutorial 3

1. Name two advantages of digital data as compared to analog data.

2. What is the period if the clock frequency is 3.5GHz.

3. Convert each binary number to decimal.

(i) 1110001.0001 (ii) 1111111.11111 (iii) 110011.11

4. Write the BCD code of decimal no.

(i) 98 (ii) 18 (iii) 156

5. Draw the OR, AND, NAND, NOR, Ex-OR and Ex-NOR gate and write its truth table.

6. (a) ADD (AB9)16 + (546)16 =_____.

(b) ADD (1101)2+(1011)2=_____.

(c) ADD BCD No. (10011000) +(10010111) =_____.

Digital Electronics (EE-041402)
Tutorial 4

1. Express each decimal number as an 8-bit number in the 2's complement form.

(i) +12 (ii) -68 (iii) +101

2. Determine which of the following even parity codes are in error:

(i) 100110010 (ii) 011101010 (iii) 10111111010001010

3. **a)** Express the following Binary function in sum of minterms and product of maxterms.
F(x, y, z)= (xy+z)(y+xz)

b) Convert the following numbers in Binary, Octal, Decimal and Hexadecimal number system?
(a) $(511)_{10}$ (2) $(ABED)_{16}$

4. **a)** What are Implicants (I), Prime Implicants (PI) and Essential Prime Implicants (EPI)? Explain with the help of example.

b) (i) Convert the Binary Code, 1111011101110 to Gray Code.

(ii) Convert the gray code 110000010001 to binary code.

5. Solve the following switching function using Quine-McCluskey Method $F(A,B,C,D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$

6. Find out they don't care elements required to minimize the expression F1=Σm(A,B,C,D,E)=A`CD` + A`BDE` + ABCDE` to F1=Σm(A,B,C,D,E)=CD` + BDE` using K-map.

Digital Electronics (EE-041402)

Assignment 1

(a) Convert the decimal number 45.5 to binary number.

(b) Convert the Gray code 10111111 to binary.

(c) Convert BCD code 1001010001110000 to decimal.

(d) Convert hexadecimal number 9B30 to decimal number.

(e) convert decimal number 359 to octal number.

2. What is combinational circuit? Explain 2 to 4 decoder with the suitable Diagram and truth table. Also realize it by using logic gates.

3. Draw the symbol of OR, AND, NAND, NOR, Ex-OR and Ex-NOR gate and write their truth table.

4. Write short notes on any two:

   (a) Gray code
   (b) Alpha numeric code
   (c) ASCII code
   (d) Excess-3 code

5. Explain Karnaugh Map (K-Map). Map the following standard expression on a Karnaugh map:
$\bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + AB\bar{C}D + ABCD + AB\bar{C}\bar{D} + A\bar{B}C\bar{D}$. Also write its all essential prime implicants.

6 State and explain DeMorgan's Theorem. Apply DeMorgan's Theorem to simplify the boolean function $\overline{(A+B)\overline{CD}+E+\overline{F}}$ into $(\overline{A}\overline{B}+C+D)\overline{E}F$.

Digital Electronics (EE-041402)

Assignment 2

1. Using Boolean algebra, simplify each expression:
   (a) $\overline{A}B+\overline{A}B\overline{C}+\overline{A}BCD+\overline{A}B\overline{C}\overline{D}E$ (b) $AB+(\overline{A}+\overline{B})C+AB$
2. Apply DeMorgan's theorems to each expression:
   (a) $\overline{(A+\overline{B}+C+\overline{D})}+\overline{(ABC\overline{D})}$ (b) $\overline{\overline{AB}(CD+\overline{E}F)(\overline{AB}+\overline{CD})}$
3. Using Signed –Magnitude Addition add -5 and +10, signed numbers, then the sum in form of Signed –Magnitude in binary
   (a) 00101 (b) 00110 (c) 10100 (d) 00100
4. Using 8's complement solve $(829)_{10}$ - $(999)_{10}$ unsigned numbers, then the solution in octal is
   (a) -170 (b) -252 (c) 7526 (d) -251
5. Dual Expression of ABC + $\bar{A}\bar{B}\bar{C}$ + $\bar{A}$BC + A$\bar{B}\bar{C}$ = _____
6. If a Function F= (A, B, C) = Σ (0, 1, 2, 7) , then $\bar{F}$ = ?
   (a) Π (3, 4, 5, 6) (b) Σ (3, 4, 5, 6) (c) Π (0, 1, 2, 7) (d) Both b and c
7. Find the complement of F = $\bar{X}$YZ + X$\bar{Y}$Z + X$\bar{Y}\bar{Z}$ i.e. $\bar{F}$ = _____

MUZAFFARPUR INSTITUTE OF TECHNOLOGY, MUZAFFARPUR
B.Tech 4th Semester Mid-Term Examination, 2018
Digital Electronics (041402)

Time: 2 hours **Full Marks: 20**

Instructions: **(i) Attempt any four questions.**
(ii) The marks are indicated in the right-hand margin.
(iii) All questions carry equal marks.

Answer the following questions

1. (a) Convert the binary number 11000110 to Gray code. **5**

   (b) Convert the Gray code 10101111 to binary.

   (c) Convert BCD code 1001010001110000 to decimal.

   (d) Convert decimal number 2469 to BCD.

   (e) Write the 2's complement of binary number 00111101.

2. Explain the basic gates and universal gates with their Truth Table and Timing Diagram. **5**

3. Convert the following numbers in Binary, Octal, Decimal and Hexadecimal number system? **5**
   (a) $(511)_{10}$ (b) $(ABED)_{16}$.

4. Explain Multiplexer with suitable block Diagram and also realise1 to 4 multiplexer with logic gates. **5**

5. (I) Add the hexadecimal numbers. **5**

   (a) $(18)_{16}+(34)_{16}$ (b) $(3F)_{16}+(2A)_{16}$.
   (II) Substract the hexadecimal numbers.
   (a) $(75)_{16}-(21)_{16}$ (b) $(94)_{16}-(5C)_{16}$.

6 State and explain DeMorgan's Theorem. Simplify the following Boolean expression $\overline{AB+AC}+\overline{A}\overline{B}C$ into $\overline{A}+\overline{B}\overline{C}$. **5**

Question Bank:

Code : 041302

2012

DIGITAL ELECTRONICS

Time : 3 hours **akubihar.com** *Full Marks* : 7(

Instructions :

(i) All questions carry equal marks.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Choose the correct answer (any *seven*) :

(a) The decimal equivalent of binary numbe 1101·0011 is

(i) 12·1875

(ii) 13·1875

(iii) 11·1865

(iv) 13·1865

(b) A full adder can be made of

(i) two half adders

(ii) two half adders and a NOR gate

(iii) two half adders and an OR gate

(iv) two half adders and an AND gate

(c) When two 16-input multiplexers drive a 2-input MUX, what is the result?

(i) 2-input MUX

(ii) 4-input MUX

(iii) 16-input MUX **akubihar.com**

(iv) 32-input MUX

(d) The 'race-around' condition occurs when

(i) $J = 0,\ K = 0$

(ii) $J = 0,\ K = 1$

(iii) $J = 1,\ K = 0$

(iv) $J = 1,\ K = 1$

(e) The maximum possible number of states in a ripple counter with 5 flip-flops is

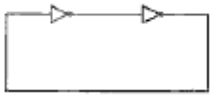
(i) 32

(ii) 15

(iii) 10

(iv) 5

(f) The digital circuit using two inverters shown in the figure will act as



(i) a bistable multivibrator

(ii) an astable multivibrator

(iii) a monostable multivibrator

(iv) an oscillator

(g) The logic circuit which belongs to non-saturated logic is

(i) ECL

(ii) TTL

(iii) CMOS

(iv) NMOS

(h) A 12-bit A/D converter has a range of 0–10 V. What is the approximate resolution of the converter?

(i) 1 mV

(ii) 2·5 mV

(iii) 2·5 μV

(iv) 12 mV

(i) Which one of the following statements about RAM is not correct?

(i) RAM stands for random access memory

(ii) It is also called read/write memory

(iii) When power supply is switched off, the information in RAM is usually lost

(iv) The binary contents are entered or stored in the RAM chip during the manufacturing

(j) The minimum number of flip-flop required to construct a mod-75 counter is

(i) 5

(ii) 6

(iii) 7

(iv) 8

  (Turn Over)

2. (a) Draw a full-adder circuit and explain its operation.

(b) Explain the general principle of counter-type A/D converter.

3. (a) State and prove de Morgan's theorem. How is it helpful in minimizing a given Boolean expression?

(b) Show that

(i) $\overline{\overline{A}+B}+\overline{\overline{A}+\overline{B}}=A$

(ii) $(A+B)(B+C)(C+A)=AB+BC+CA$

(iii) $AB+\overline{B}\,\overline{C}+A\overline{C}=AB+\overline{B}\,\overline{C}$

(c) Simplify $B+A\overline{B}+AB$.

4. (a) What is *J-K* flip-flop? How can problems associated with *R-S* flip-flop be eliminated with the help of *J-K* flip-flop?

(b) Design a 3-bit synchronous counter using *J-K* flip-flops.

5. (a) How do you realise a parity bit checker?

(b) Describe the operation of the parallel in serial out shift register with neat logic diagram.

6. Design a mod-8 up-down counter.

  (Continued)

Code : 041302

B.Tech 3rd Semester Exam., 2015

DIGITAL ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Choose the correct option of the following (any *seven*) : 2×7=14

(a) Universal gate is

(i) AND gate

(ii) OR gate

(iii) NAND gate

(iv) XOR gate

(b) Number of minimum 2-input NAND gates required to make half-adder circuit is

(i) 2

(ii) 3

(iii) 4

(iv) 5

7. *(a)* Design a 100 kHz, 60% duty cycle square wave generator using 555 timer.

(b) A D/A converter has a full-scale analog output of 10 V and accepts six binary bits as inputs. Find the voltage corresponding to each analog step.

8. A digital system has four bits of a 4-bit word *ABCD* as inputs. The output *Y* is equal to 1 when any two adjacent bits are 1, or any three or all four bits are 1.

(a) Draw the Karnaugh map for *Y*.

(b) Realise *Y* using 2-input and 3-input NAND gates only.

9. Write short notes on the following :

(a) EEPROM

(b) DTL logic

(c) Race-around condition

(d) Encoders

(c) Which one of the following is a sequential circuit?

(i) Mux

(ii) Half-adder

(iii) Demux

(iv) Flip-flop

(d) Which one of the following circuits is a combinational circuit?

(i) Counter

(ii) Register

(iii) Memory

(iv) Mux

(e) Number of flip-flop required to make modulo-6 counter is

(i) 1

(ii) 2

(iii) 3

(iv) 4

(f) Combinational circuit output depends upon

(i) present input

(ii) present output

(iii) previous output

(iv) None of the above

(g) Sequential circuit output depends upon

(i) present input and previous output

(ii) present input and present output

(iii) only present input

(iv) None of the above

(h) For the design of one full-adder circuit, the required number of half-adder is

(i) 1

(ii) 2

(iii) 3

(iv) 4

2. (a) Draw the circuit diagram of full-adder circuit using NAND gates. 6

(b) Draw and explain the circuits of monostable and bistable multivibrators. 8

3. (a) Draw the circuit diagram of 1 : 8 demux and explain. 6

(b) Design priority encoder and explain the circuit with suitable truth table. 8

4. (a) Draw the circuit diagram of 2-input NAND gate using CMOS logic and explain the switching action of the transistors. 6

(b) Explain the differences between TTL and CMOS logic. 8

Code : 041402

B.Tech. 4th Semester Exam., 2014

DIGITAL ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) *The marks are indicated in the right-hand margin.*

(ii) *There are* ***NINE*** *questions in this paper.*

(iii) *Attempt* ***FIVE*** *questions in all.*

(iv) *Question No. 1 is compulsory.*

1. Choose the correct option from the following (any *seven*) : 2×7=14

(a) A quantity having continuous wave is

(i) a digital quantity

(ii) an analog quantity

(iii) a binary quantity

(iv) a natural quantity

(b) The sum of $11010_2 + 01111_2$ equals

(i) 101001

(ii) 101010

(iii) 110101

(iv) 101000

(c) The output of a gate is low if and only if its input are HIGH. It is true for

(i) AND

(ii) XNOR

(iii) NOR

(iv) NAND

(d) An example of a standard SOP expression is

(i) $\overline{A}\overline{B} + A\overline{B}C + A\overline{B}\overline{D}$

(ii) $A\overline{B}C + ACD$

(iii) $A\overline{B} + \overline{A}B + AB$

(iv) $AB\overline{C}D + \overline{A}B + \overline{A}$

(e) To implement the expression of $\overline{A}BCD + A\overline{B}CD + AB\overline{C}\overline{D}$, it takes one OR gate and

(i) one AND gate

(ii) three AND gates

(iii) three AND gates and four inverters

(iv) three AND gates and three inverters

(f) The invalid state of an *S-R* latch occurs when

(i) $S = 1, R = 0$

(ii) $S = 0, R = 1$

(iii) $S = 1, R = 1$

(iv) $S = 0, R = 0$

(Continued)

5. (a) Design a full adder using only NAND gate. 7

(b) Design a 8 to 1 line multiplexer using 4 to 1 line multiplexer. 7

6. (a) Differentiate between synchronous and asynchronous counter. 7

(b) Design a 4-bit synchronous up counter. 7

7. (a) Explain the following flip-flops with their diagrams and truth tables : 7

(i) SR F/F

(ii) J-K F/F

(iii) D F/F

(iv) T F/F

(b) Design D F/F from J-K F/F. 7

8. (a) Explain the working principle of a successive approximation ADC with the help of circuit diagram. 7

(b) Find the output voltage from a 5-bit ladder D/A converter which has a digital input of 11010. Assume 0 = 0 V and 1 = +10 V. 7

9. Write short notes on any *two* of the following : 7×2=14

(a) Data transfer in a shift register

(b) ROM

(c) Astable multivibrator using 555

(d) Digital comparator

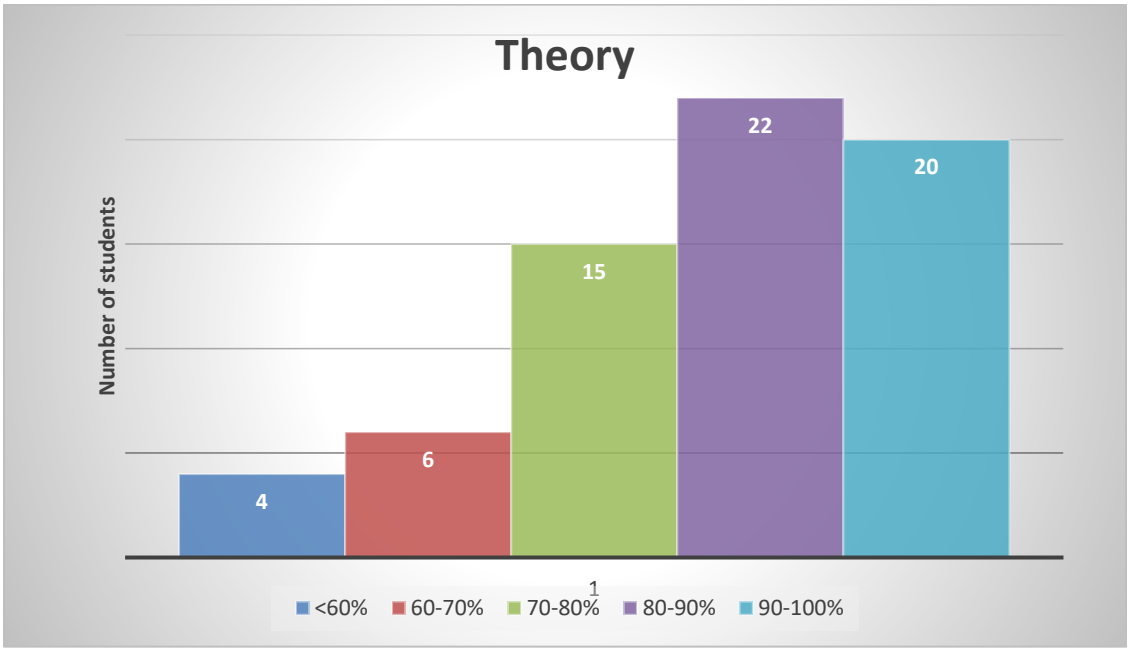
Result of the students

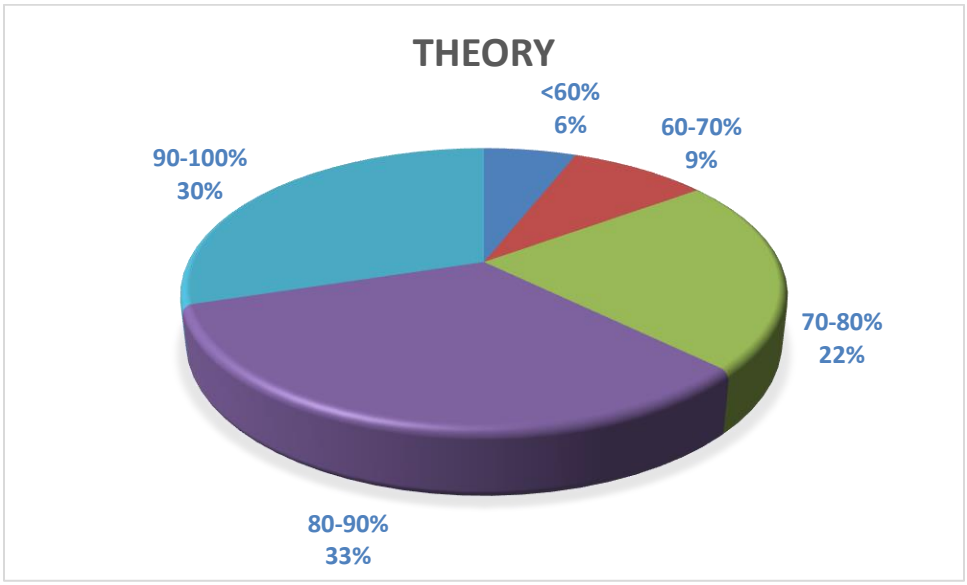
Roll No	Name	Theory				Practical			
		Marks of attendance	Class test	Mid semester exam	Total	Marks of attendance	Class performance	viva voice	Total
16EE02	ANJALI KUMARI	5	5	18	28	5	5	10	20
16EE03	KAUSTUBHA	5	5	16	26	5	5	9	19
16EE05	AMRITA KUMARI	5	5	12	22	5	5	8	18
16EE06	SUMIT KUMAR	5	5	15	25	5	5	8	18
16EE07	RITESH RAJ	5	5	17	27	5	5	8	18
16EE08	VIPUL MISHRA	5	5	14	24	5	5	8	18
16EE10	MD SAIFULLAH SADIQUE	5	5	15	25	5	5	8	18
16EE11	PREETI KUMARI	5	5	11	21	5	5	7	17
16EE12	KULDEEP THAKUR	5	5	10	20	5	5	8	18
16EE13	SHANTANU SINGH	5	5	17	27	5	5	8	18
16EE14	SEEMA KUMARI	5	5	15	25	5	5	8	18
16EE15	PRIYAM KUMARI	5	5	20	30	5	5	10	20
16EE16	VANDANA BIHARI	5	5	16	26	5	5	7	17
16EE17	RAJNANDANI	5	5	17	27	5	5	7	17
16EE18	SANJAY KUMAR	5	5	19	29	5	5	10	20
16EE19	PRAVEEN DIVAKAR	5	5	19	29	5	5	10	20
16EE20	AMIT KUMAR PANDIT	5	5	0	10	5	5	10	20
16EE21	CHANDAN KUMAR THAKUR	5	5	11	21	5	5	7	17
16EE22	ALOK KUMAR	5	5	14	24	5	5	8	18
16EE23	DEVENDRA KUMAR	5	5	14	24	5	5	8	18

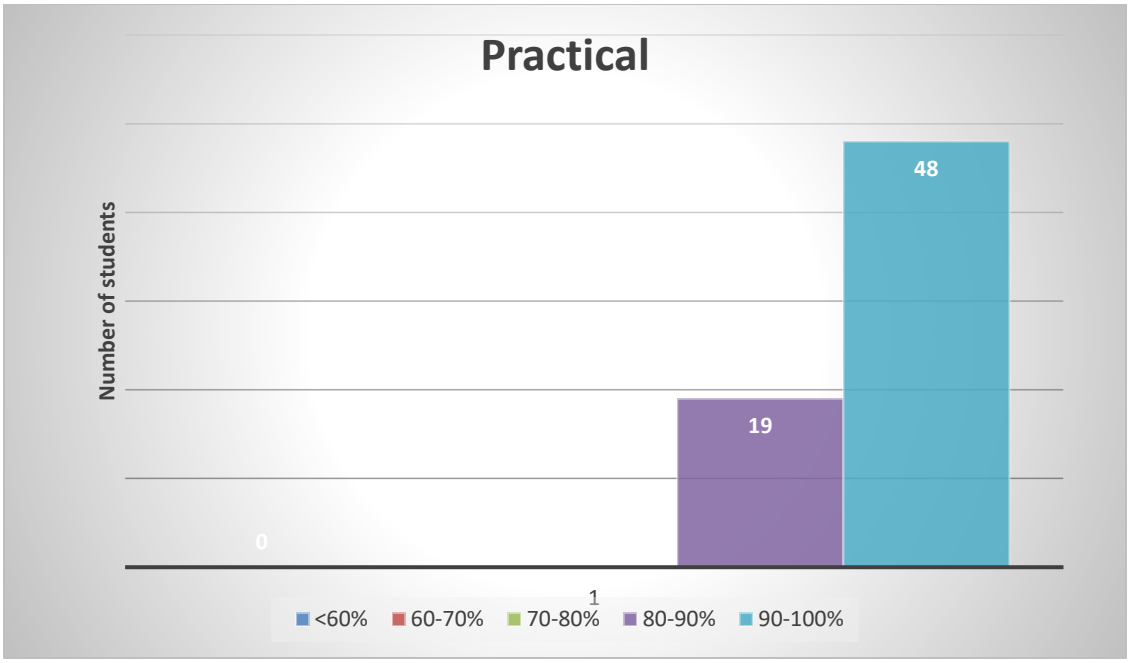
16EE24	ARVIND KUMAR	5	5	11	21	5	5	7	17
16EE25	AMITESH KUMAR	5	5	17	27	5	5	7	17
16EE26	VIVEK KUMAR	5	5	16	26	5	5	8	18
16EE27	VIKASH KUMAR RAY	5	5	11	21	5	5	7	17
16EE28	ROHIT KUMAR	5	5	14	24	5	5	8	18
16EE30	RAVI KUMAR	5	5	18	28	5	5	7	17
16EE31	SANDEEP KUMAR	5	5	15	25	5	5	10	20
16EE32	DEO ALOK	5	5	18	28	5	5	10	20
16EE33	BAJRANGI KUMAR	5	5	18	28	5	5	10	20
16EE34	MANOJ KUMAR SONI	5	5	12	22	5	5	8	18
16EE36	NEERAJ KUMAR	5	5	15	25	5	5	8	18
16EE39	NITISH KUMAR RAJAK	5	5	15	25	5	5	7	17
16EE40	UJJAWAL KUMAR	5	5	9	19	5	5	7	17
16EE41	PRABHAT KUMAR	5	5	13	23	5	5	7	17
16EE42	MD HASIM JILANI	5	5	5	15	5	5	7	17
16EE44	ANISH BHARTI	5	5	13	23	5	5	8	18
16EE45	RAHUL KUMAR	5	5	15	25	5	5	8	18
16EE46	RAJEEV RANJAN PRASAD	5	5	5	15	5	5	7	17
16EE49	PRASHANT KUMAR	5	5	16	26	5	5	8	18
16EE50	NAMAN KUMAR	5	5	10	20	5	5	7	17
16EE51	KESHAV CHANDRA	5	5	16	26	5	5	9	19
16EE52	SWETA BHARTI	5	5	17	27	5	5	9	19
16EE53	PRATIK ANAND	5	5	14	24	5	5	8	18
16EE54	SHAGUFTA ANJUM	5	5	20	30	5	5	10	20
16EE55	GOLDEN KUMAR	5	5	11	21	5	5	8	18

16EE56	MURLI MANOHAR	5	5	16	26	5	5	10	20
16EE57	ARPIT ANAND	5	5	8	18	5	5	7	17
16EE58	AKSHAT RAJ	5	5	13	23	5	5	7	17
16EE59	ANJAN KUMAR	5	5	17	27	5	5	9	19
16EE60	SUMAN KUMAR BHARTIYA	5	5	16	26	5	5	8	18
16EE61	SAKET	5	5	12	22	5	5	8	18
16EE62	RISHABH KUMAR	5	5	18	28	5	5	9	19
16EE63	SUMAN KUMAR	5	5	16	26	5	5	8	18
16EE64	SUNITA KUMARI	5	5	18	28	5	5	9	19
16EE65	NISHANT RAJ	5	5	16	26	5	5	9	19
16EE66	VIPIN SINGH	5	5	13	23	5	5	8	18
16EE67	ANKIT RAJ	5	5	6	16	5	5	7	17
16EE68	GUNJAN KUMAR	5	5	8	18	5	5	7	17
16EE69	PRATAP CHANDRA CHOUDHARY	5	5	13	23	5	5	7	17
17(LE)EE01	VIVEK KUMAR	5	5	16	26	5	5	10	20
17(LE)EE02	RITIK KUMAR	5	5	13	23	5	5	10	20
17(LE)EE03	ANAND RANJAN	5	5	19	29	5	5	10	20
17(LE)EE04	ABHISHEK KUMAR	5	5	13	23	5	5	10	20
17(LE)EE05	POONAM KUMARI	5	5	19	29	5	5	10	20
17(LE)EE06	SAURABH KUMAR JHA	5	5	18	28	5	5	10	20
17(LE)EE07	Parmanand Kumar	5	5	18	28	5	5	10	20
17(LE)EE08	ROHAN RAJ	5	5	8	18	5	5	10	20
17(LE)EE09	ANAND KUMAR	5	5	18	28	5	5	10	20
17(LE)EE10	MANISH	5	5	13	23	5	5	10	20

RESULT ANALYSIS






Practical
Number of students
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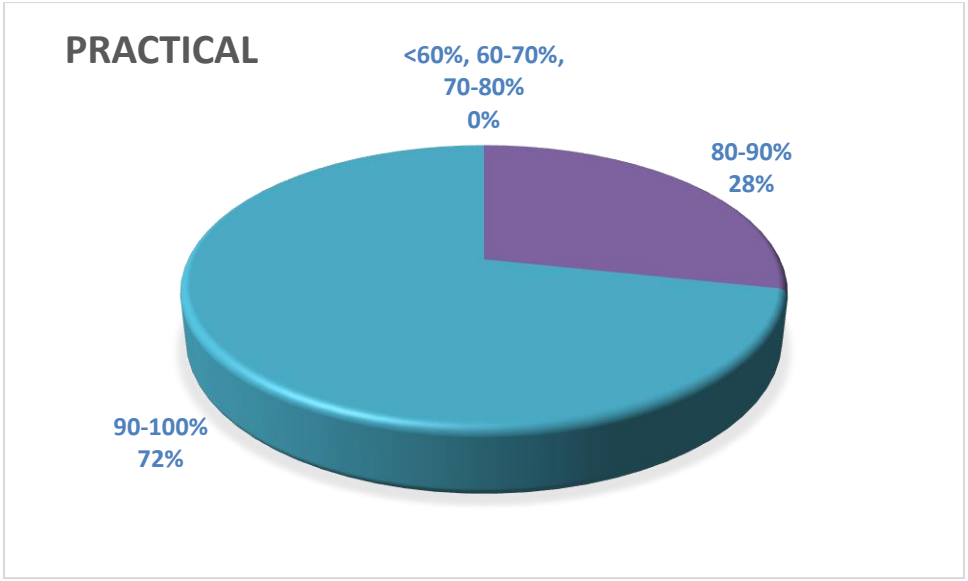
60-70%
70-80%
80-90%
90-100%


PRACTICAL
<60%, 60-70%,
70-80%
0%
80-90%
28%
90-100%
72%