MUZAFFARPUR INSTITUTE OF TECHNOLOGY, MUZAFFARPUR, BIHAR – 842003

(Under the department of Science & Technology, Bihar, Patna)

B.Tech 3rd Semester Mid-Term Examination, 2018
Digital Electronics

Solution

Q.N. 1(a) convert the decimal number $(37.625)_{10}$ into binary number $(\ )_2$.

Sol^n:- The decimal number 37.625 contains integer part 37 and fraction part 0.625.

conversion of integer part :- (Division operation by 2)

			Generated Remainder
2	37		
2	18	→	1
2	9	→	0
2	4	→	1
2	2	→	0
2	1	→	0
	0	→	1

Thus, $(37)_{10} = (100101)_2$

conversion of fractional part :- (Multiplication operation by 2)

		Generated Integer
0.625×2	$= 1.250$ →	1
0.250×2	$= 0.500$ →	0
0.500×2	$= 1.000$ →	1

Thus, $(0.625)_{10} = (101)_2$

combindly, $(37.625)_{10} = (100101.101)_2$

1(b) Determine the 2's complement of the number $(1010111)_2$

Sol^n:- 2's complement of the binary number can be obtained by first taking 1's complement and then adding 1 to it.

1 0 1 0 1 1 1
↓ ↓ ↓ ↓ ↓ ↓ ↓
0 1 0 1 0 0 0 → 1's complement (complementing 1 to 0 & 0 to 1)

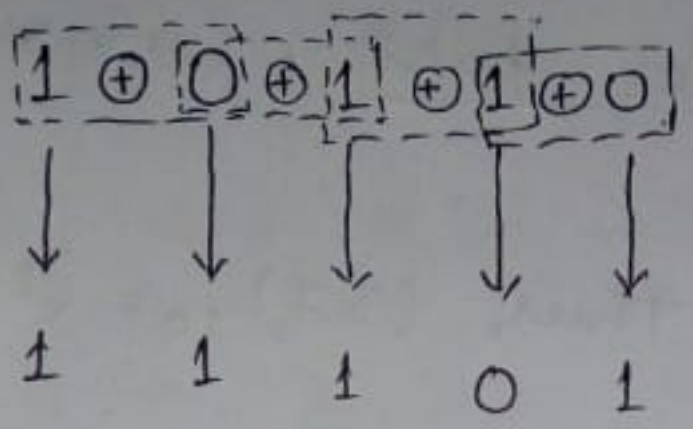
$+$ 1

0 1 0 1 0 0 1 → 2's complement

Thus, 2's complement is $(0101001)_2$.

1(c) convert the binary number $(10110)_2$ into Gray code.

Sol^n:- Binary to Gray code conversion



Thus, the Gray code is $(1\,1\,1\,0\,1)_G$.

1(d) Perform the binary subtraction 11110 − 11011.

Sol^n:- Binary subtraction:-

$$\begin{array}{r} 1\ 1\ 1\ 1\ 0 \\ 1\ 1\ 0\ 1\ 1 \\ \hline 0\ 0\ 0\ 1\ 1 \end{array}$$

Thus, the result after subtraction $(00011)_2$

1(e) Add the BCD number 1001 & 0100

Sol^n:-

$$\begin{array}{r} 1\ 0\ 0\ 1 \\ +\ 0\ 1\ 0\ 0 \\ \hline 1\ 1\ 0\ 1 \end{array}$$

→ The decimal equivalent of this BCD is greater than 9, therefore it is not a valid BCD number. Therefore we will add $(0110)_2$ to skip the six invalid states.

$$\begin{array}{r} 1\ 1\ 0\ 1 \\ 0\ 1\ 1\ 0 \\ \hline 0\ 0\ 0\ 1\ \ 0\ 0\ 1\ 1 \end{array}$$

The three zeros are added to make a 4 bit binary number.

(0001 0011). Ans

Q.N. 2(a) Using Boolean theorem prove that

$$A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D = A+B+C+D$$

Sol^n:-

$$A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D$$

$$= (A+\bar{A})(A+B) + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D$$ (using distributive property $A + BC = (A+B)\cdot(A+C)$)

$$= A+B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D \quad (\because A+\bar{A}=1)$$

$$= B + A + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D$$ (using distributive prop)

$$= B + A + \bar{B}C + \bar{A}\bar{B}\bar{C}D$$

$$= A + B + \bar{B}C + \bar{A}\bar{B}\bar{C}D$$

$$= A + (B+\bar{B})(B+C) + \bar{A}\bar{B}\bar{C}D$$

$$= A+B+C + \bar{A}\bar{B}\bar{C}D$$

$$= B+C+A+\bar{A}\bar{B}\bar{C}D$$

$$= B+C+(A+\bar{A})(A+\bar{B}\bar{C}\bar{D})$$

$$= B+C+A+\bar{B}\bar{C}D$$

$$= A+C+B+\bar{B}\bar{C}D$$

$$= A+C+(B+\bar{B})(B+\bar{C}D)$$

$$= A+C+B+\bar{C}D$$

$$= A+B+C+\bar{C}D$$

$$= A+B+(C+\bar{C})(C+D)$$

$$= A+B+C+D$$

Proved

Q.N. 2(b) Simplify the logical expression $Y = \Sigma_m(1, 5, 10, 11, 12, 13, 15)$ using K-map and realize the simplified expression using logic gates.

Solution:

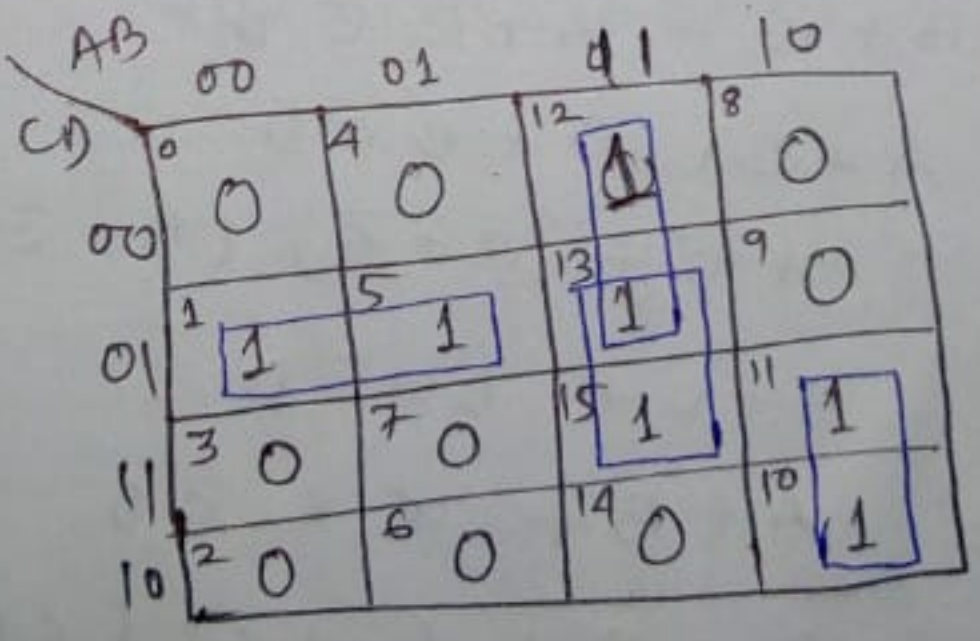
$$Y = \Sigma_m(1, 5, 10, 11, 12, 13, 15)$$

The K-map for the above expression.

CD \ AB	00	01	11	10
00	0 (0)	0 (4)	1 (12)	0 (8)
01	1 (1)	1 (5)	1 (13)	0 (9)
11	0 (3)	0 (7)	1 (15)	1 (11)
10	0 (2)	0 (6)	0 (14)	1 (10)

There are two possible ways ~~to~~ of grouping the 1's and the two expressions obtained are logically equivalent.

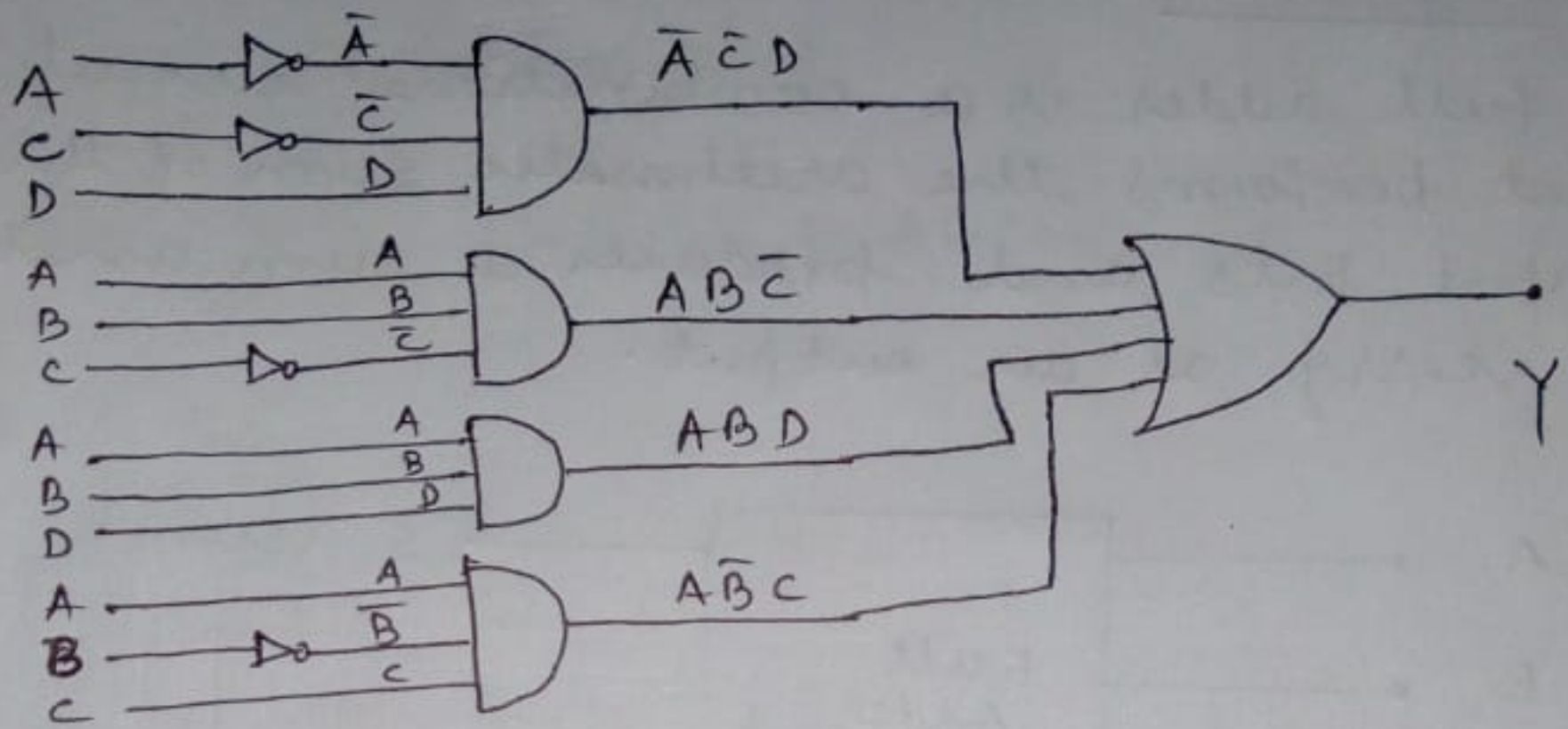
WAY-I



Simplified logical expression

$$Y = \bar{A}\bar{C}D + AB\bar{C} + ABD + A\bar{B}C$$

Realization of simplified logical expression using logic gates.

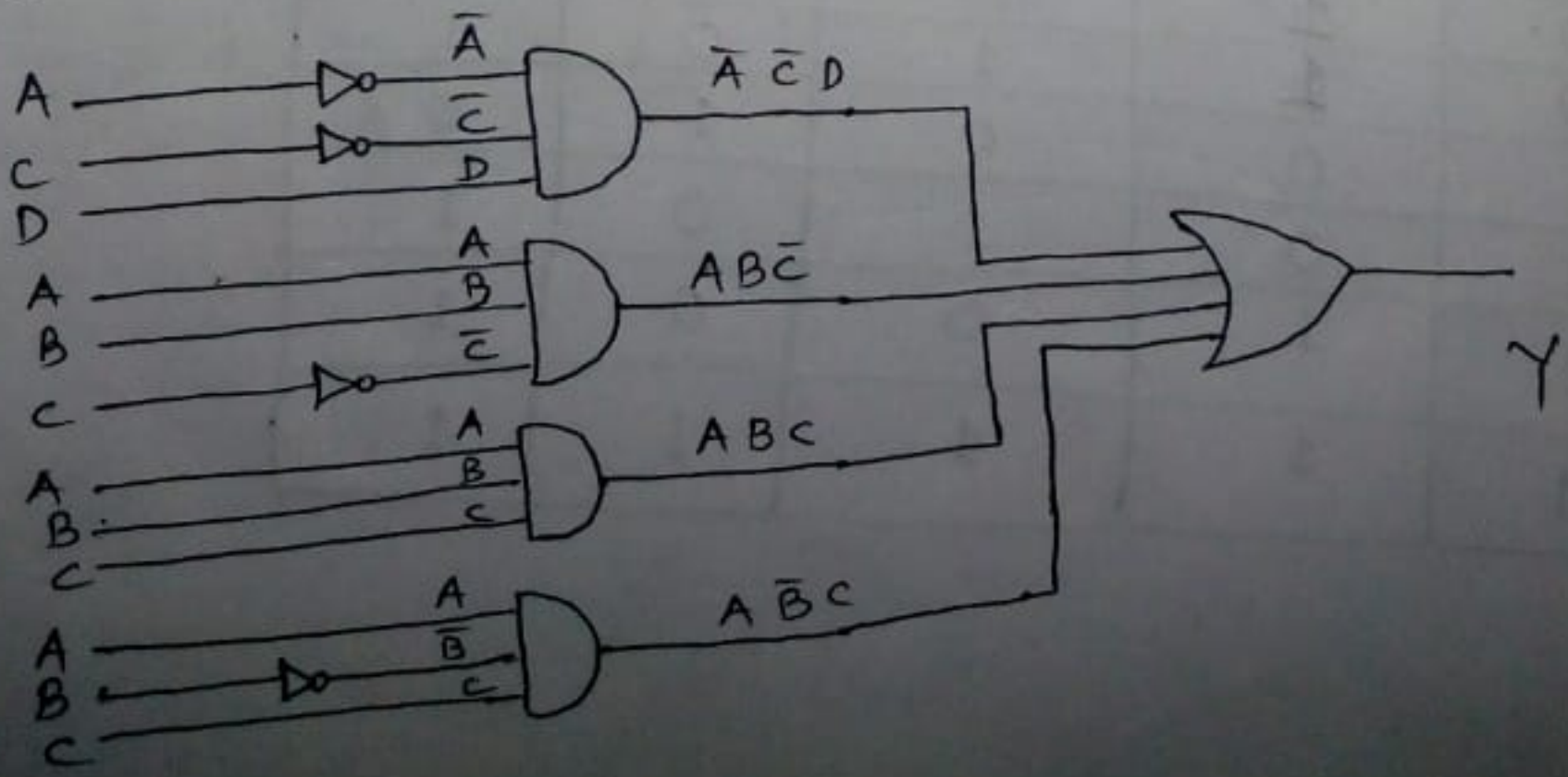


WAY-2

CD \ AB	00	01	11	10
00	0	4 0	12 1	8 0
01	1 1	5 1	13 1	9 0
11	3 0	7 0	15 1	11 1
10	2 0	6 0	14 0	10 1

$$Y = \bar{A}\bar{C}D + AB\bar{C} + ABC + A\bar{B}C$$

Realization of simplified logical expression using logic gates.

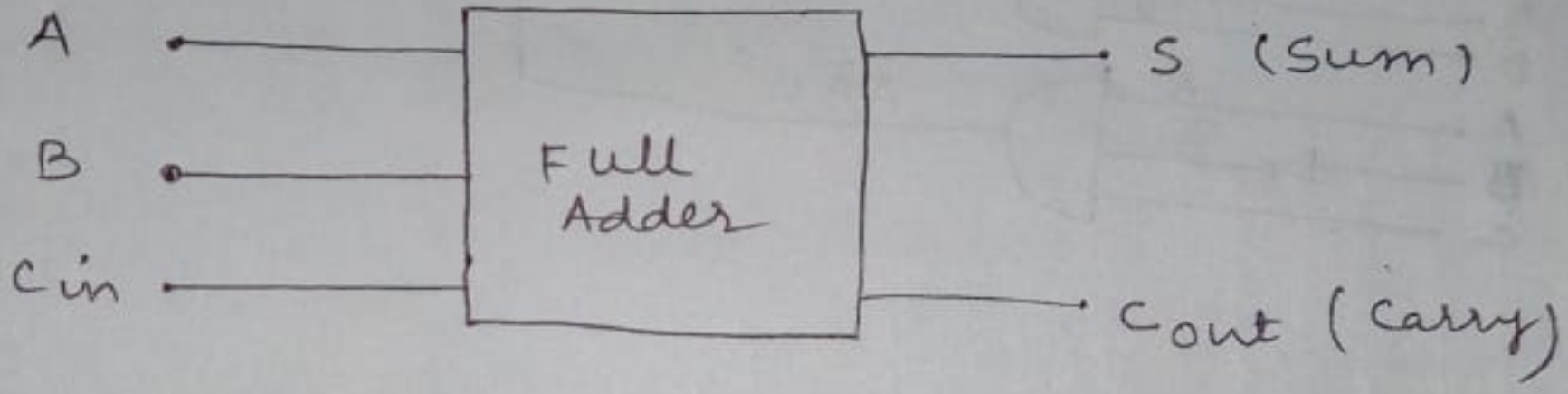


Q.N.3 (a) What is full adder? Show with the block diagram.

Solution:-

Full adder :-

A full adder is a combinational circuit that performs the arithmatic sum of three input bits and produces a sum and a carry as an output.



3(b) Write the truth table for the full adder and derive the simplified logical expressions for the sum & carry outputs.

Sol:- Truth Table of full adder

Inputs			Outputs	
A	B	Cin	Sum(S)	Carry (Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Simplified expressions of sum and carry outputs can be obtained by solving K-map for Sum (S) and carry (Cout) outputs from truth table.

Simplification for sum (S) output

AB / Cin	00	01	11	10
0	0 (0)	1 (2)	0 (6)	1 (4)
1	1 (1)	0 (3)	1 (7)	0 (5)

$$S = \bar{A}B\bar{C}in + \bar{A}\bar{B}Cin + AB Cin + A\bar{B}\bar{C}in$$

This expression can also be expressed as

$$S = (\bar{A}\bar{B} + AB)\,Cin + (\bar{A}B + A\bar{B})\,\overline{Cin}$$

$$= \overline{(A \oplus B)}\,Cin + (A \oplus B)\,\overline{Cin}$$

$$S = A \oplus B \oplus Cin$$

Simplificatin for Carry (Cout) Output

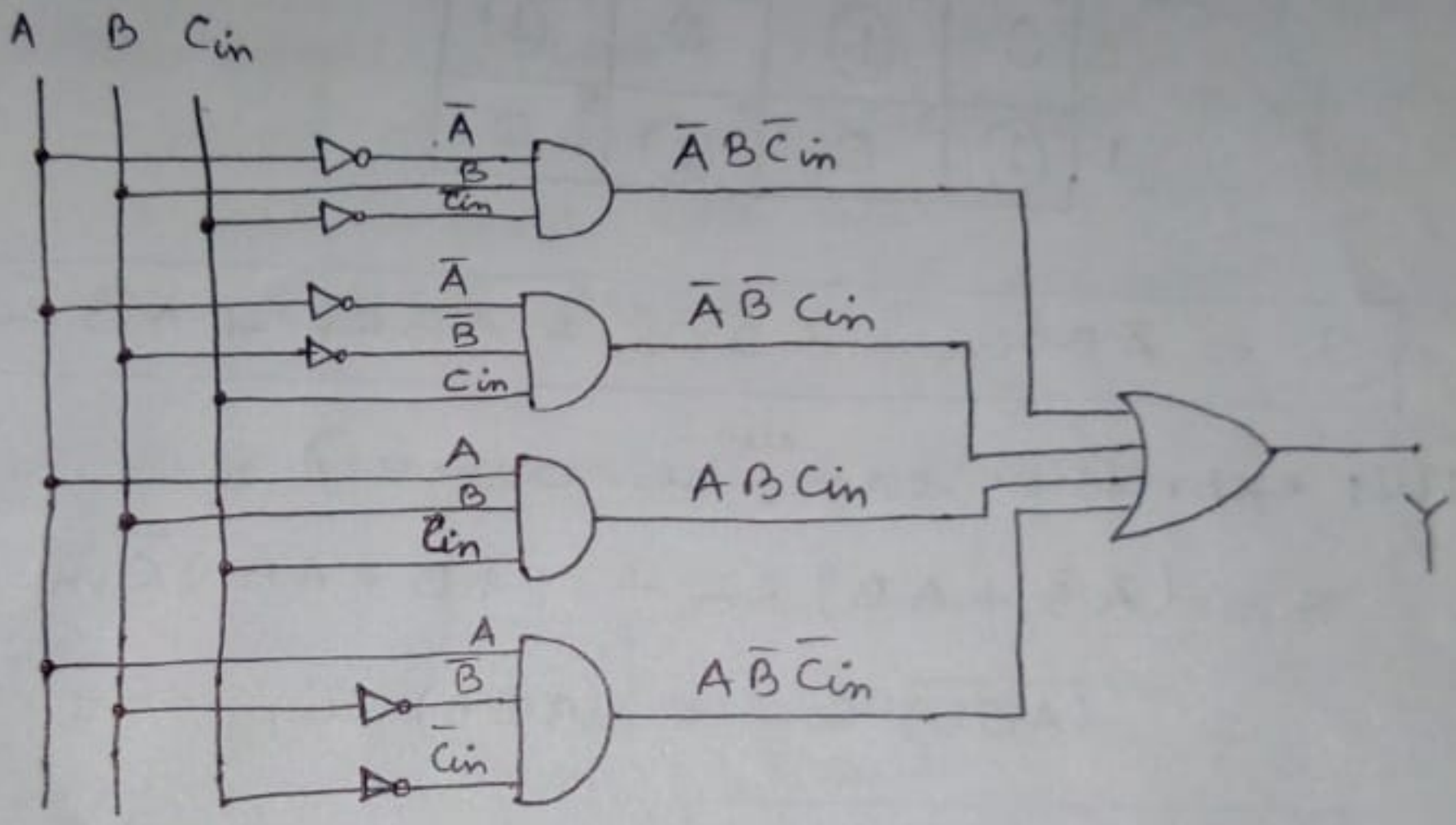
AB / Cin	00	01	11	10
0	0 (0)	0 (2)	1 (6)	0 (4)
1	0 (1)	1 (3)	1 (7)	1 (5)

$$Cout = AB + BCin + ACin$$

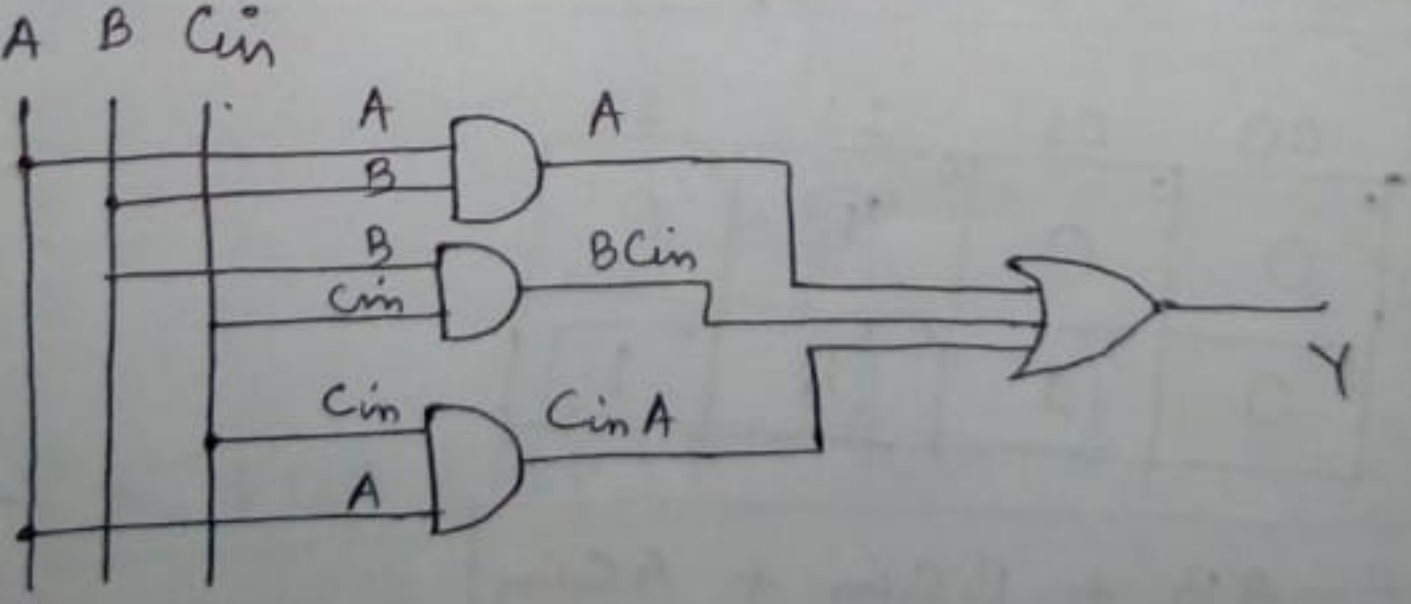
Realization of logical expressions using logic gates.

For Sum (S) output

$$S = \bar{A}B\bar{C}in + \bar{A}\bar{B}Cin + AB\,Cin + A\bar{B}\bar{C}in$$



For carry output (cout): Cout = AB + BCin + CinA



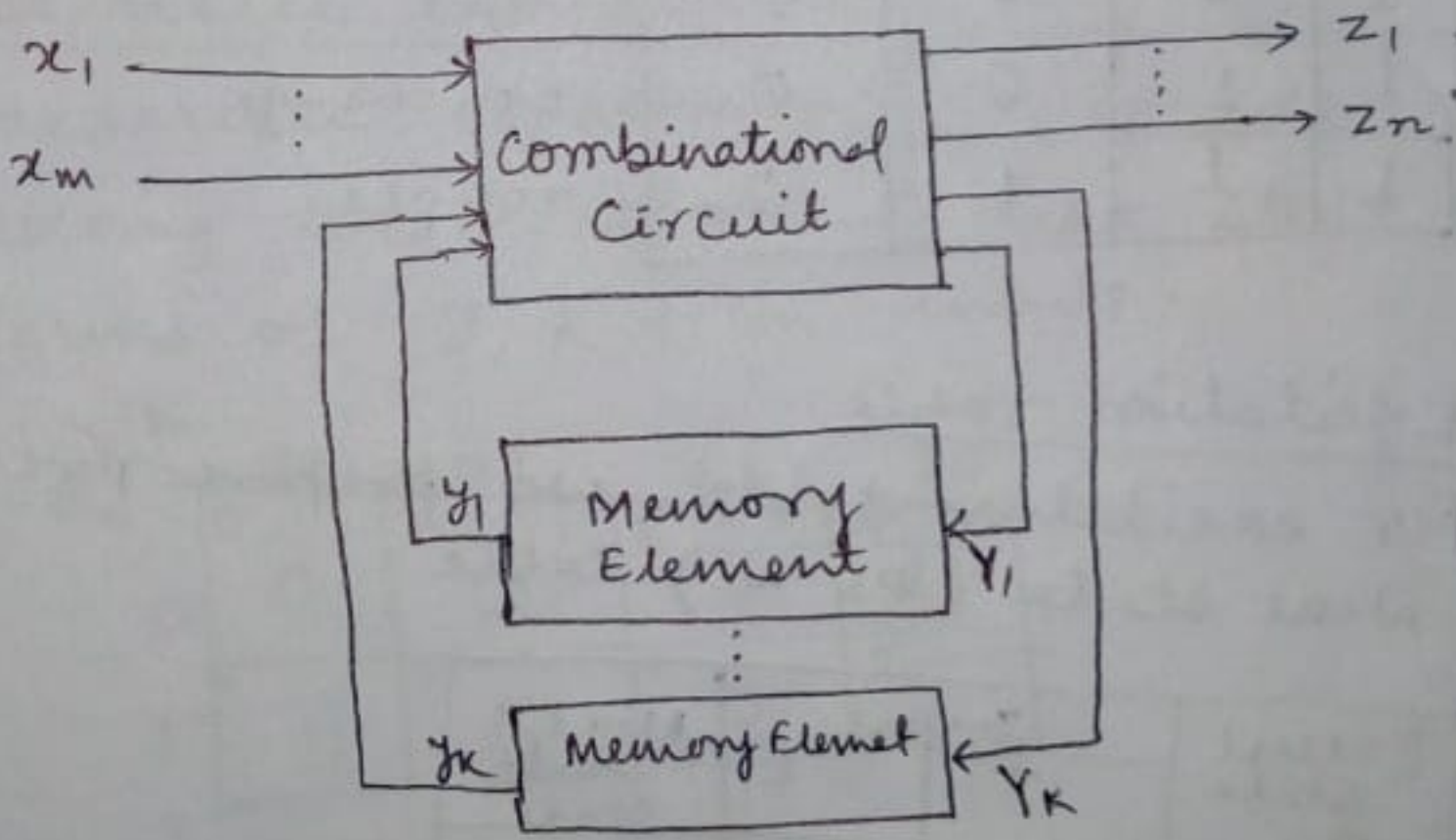
Q.N. 4(a) What is Sequential circuit? Show the block diagram, truth table, and excitation table of the JK flip flop (FF) and derive the characteristics equation.

Sol:-

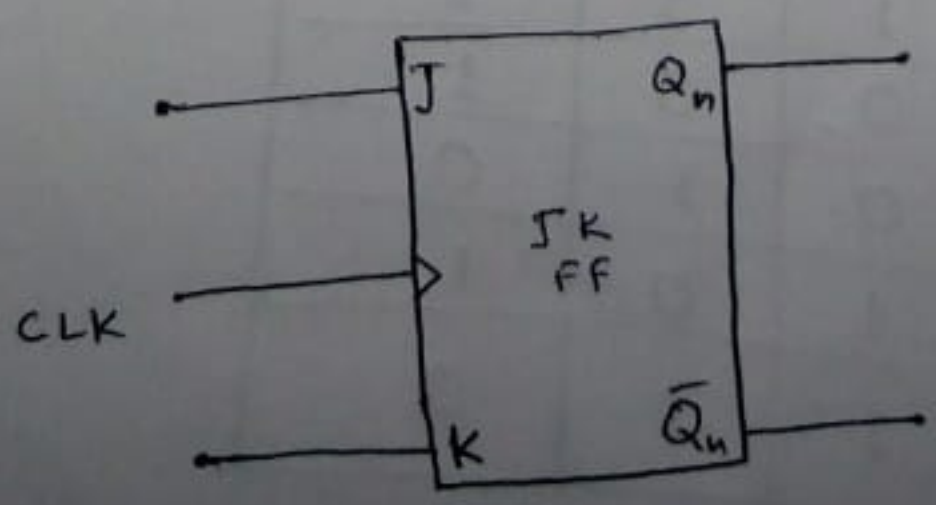
Sequential circuit :-

The logic circuit whose outputs at any instant of time depend not only on the present inputs but also on the past outputs are called sequential circuits.

Block diagram of sequential circuit



JK Flip flop (FF) :-



Block diagram of JK ff.

In the JK ff, J, K and CLK are the inputs and Q_n and $\bar{Q}_n$ are, outputs. Qn represent the present state, while after applying J, K and clk inputs the next state is represented by Q_{n+1}.

Truth Table

Inputs			Output	
J	K	CLK	Q_{n+1}	
0	0	0	Q_n	→ No change
0	0	1	Q_n	→ NO change
0	1	0	Q_n	→ No change
0	1	1	0	→ Reset
1	0	0	Q_n	→ NO change
1	0	1	1	→ set
1	1	0	Q_n	→ No change
1	1	1	$\overline{Q_n}$	→ Toggle

Excitation Table

For excitation table, we prepare present state -Next state (PS-NS) table

Present State Q_n	Inputs J	Inputs K	Next State Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation Table :-

Q_n	Q_{n+1}	Excitation I/Ps	
		J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

Excitation table is prepared from PS-NS table. we prepare a combination of I/Ps for which a particular transition in PS to next State (NS) occurs.

for example

$Q_n \to 0$ to $Q_{n+1} \to 0$ occurs in PS-NS table for the combination of J & K I/Ps as

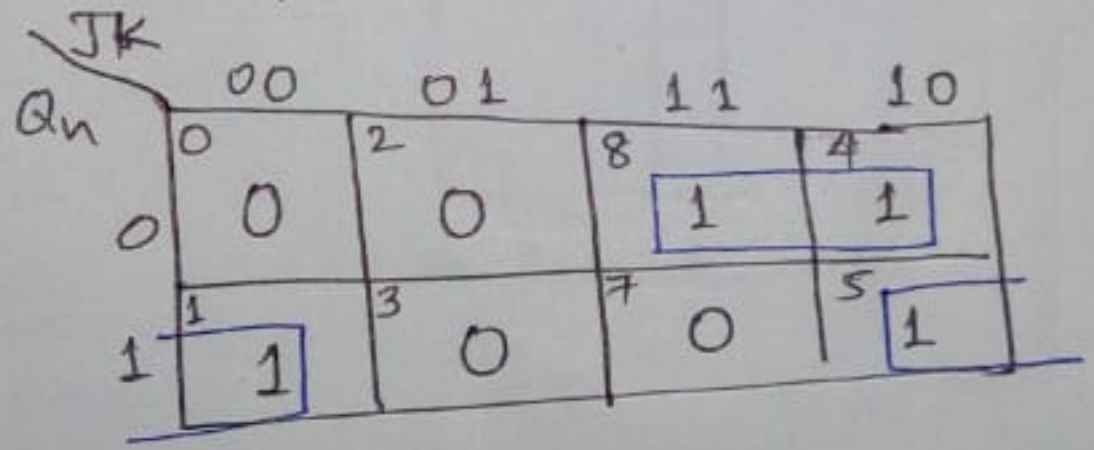
$J = 0, K = 0$ &

$J = 0, K = 1$

for $K = 0$ & 1 we take 'd'

Characteristic Equation :-

characteristic equation of JK ff can be obtained by solving the K-map for next state Q_{n+1} in terms of J, K & Q_n inputs.



$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

Q.N. 4(b) What is multiplexer (MUX)? Show with block diagram.

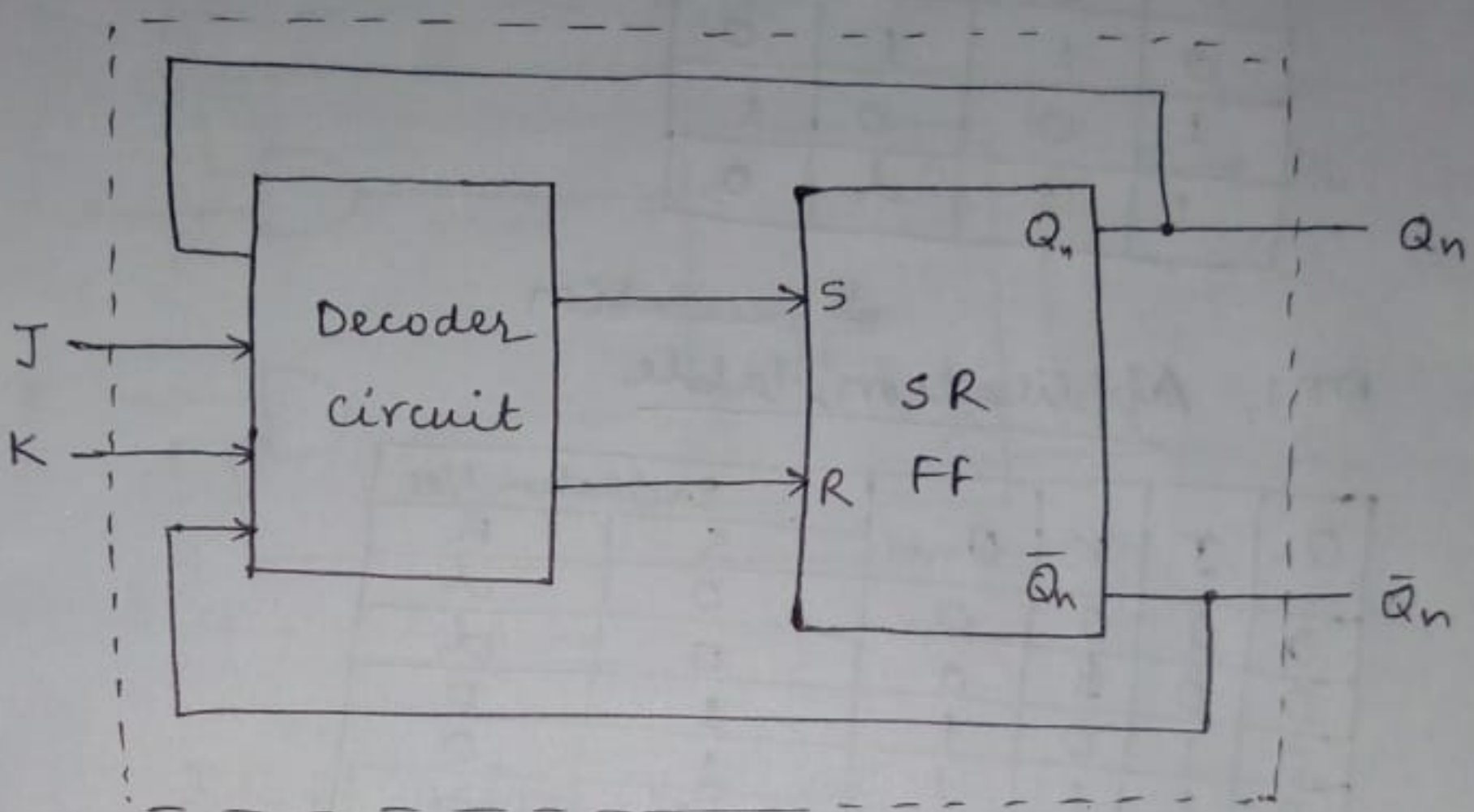
Sol^n:- **Multiplexer (MUX):-**

A digital multiplexer is a combinational circuit that selects one digital information from several sources and transmits the selected information on a single output line.

Block diagram:-

Q.N.5 (a) Realize JK Flip flop (FF) using SR flipflop (FF).

Sol:- Here, the desired ff is JK FF using the available ff, SR ff.



Block diagram of JK ff using SR FF.

First of all, the PS-NS table for JK ff is prepared.

PS-NS Table for Jk ff.

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation table of S-R ff

Q_n	Q_{n+1}	Excitation I/Ps	
		S	R
0	0	0	d
0	1	1	0
1	0	0	1
1	1	d	0

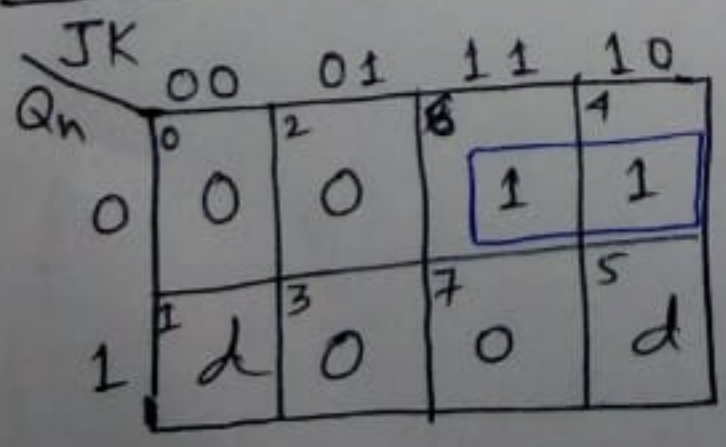
OR Excitation

Now, Application table

Q_n	J	K	Q_{n+1}	Excitation I/Ps	
				S	R
0	0	0	0	0	d
0	0	1	0	0	d
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	d	0
1	0	1	0	0	1
1	1	0	1	d	0
1	1	1	0	0	1

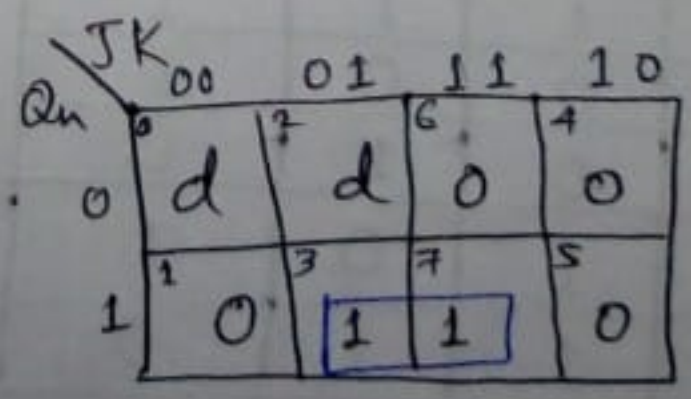
Now, For designing the decoder circuit, Simplified expressions of S & R are obtain using k-map.

For S:



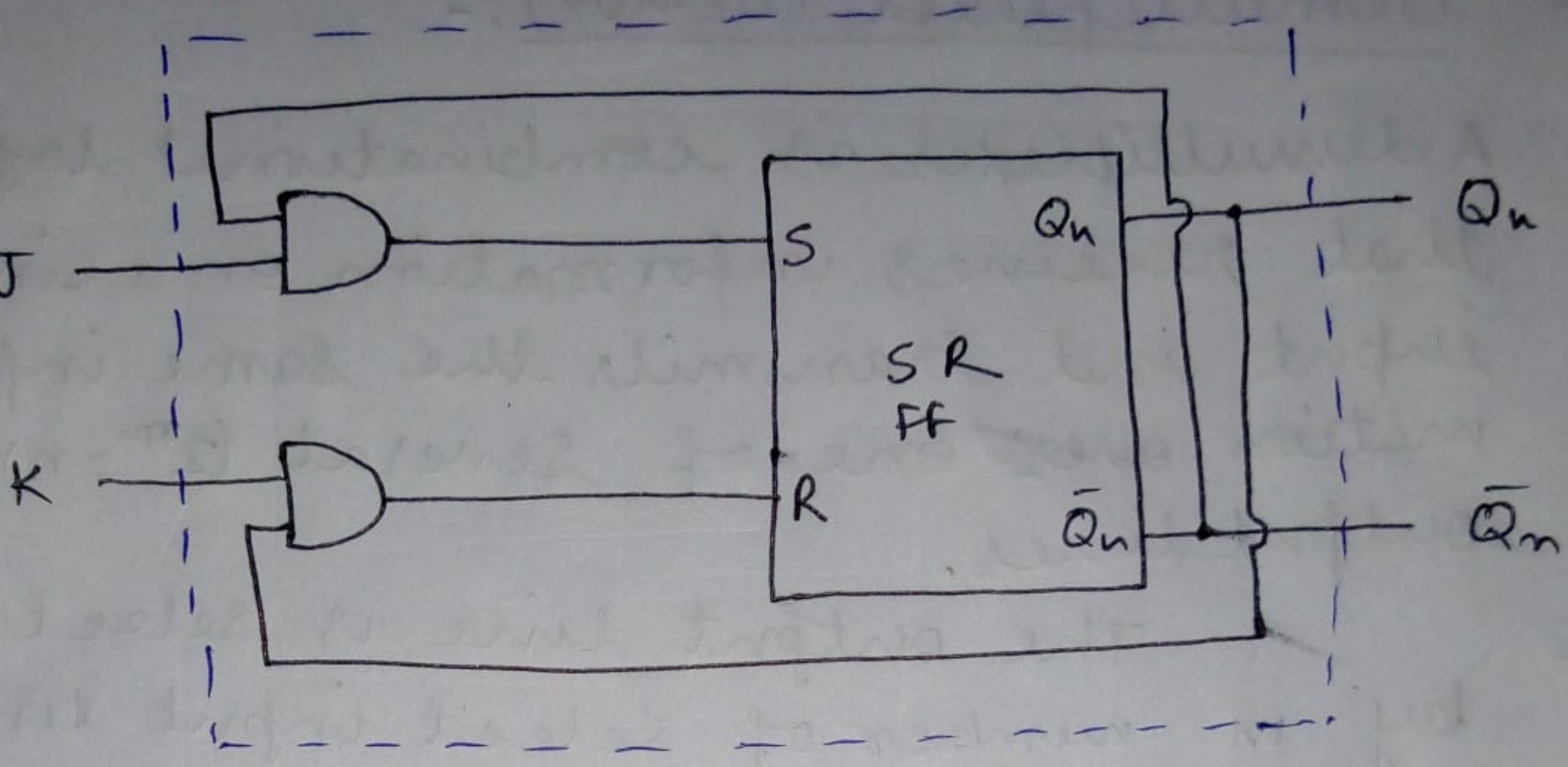
$S = J\bar{Q}_n$

For R



$R = KQ_n$

Thus, the realized JK FF using SR FF can be shown as below



JK FF using SR ff

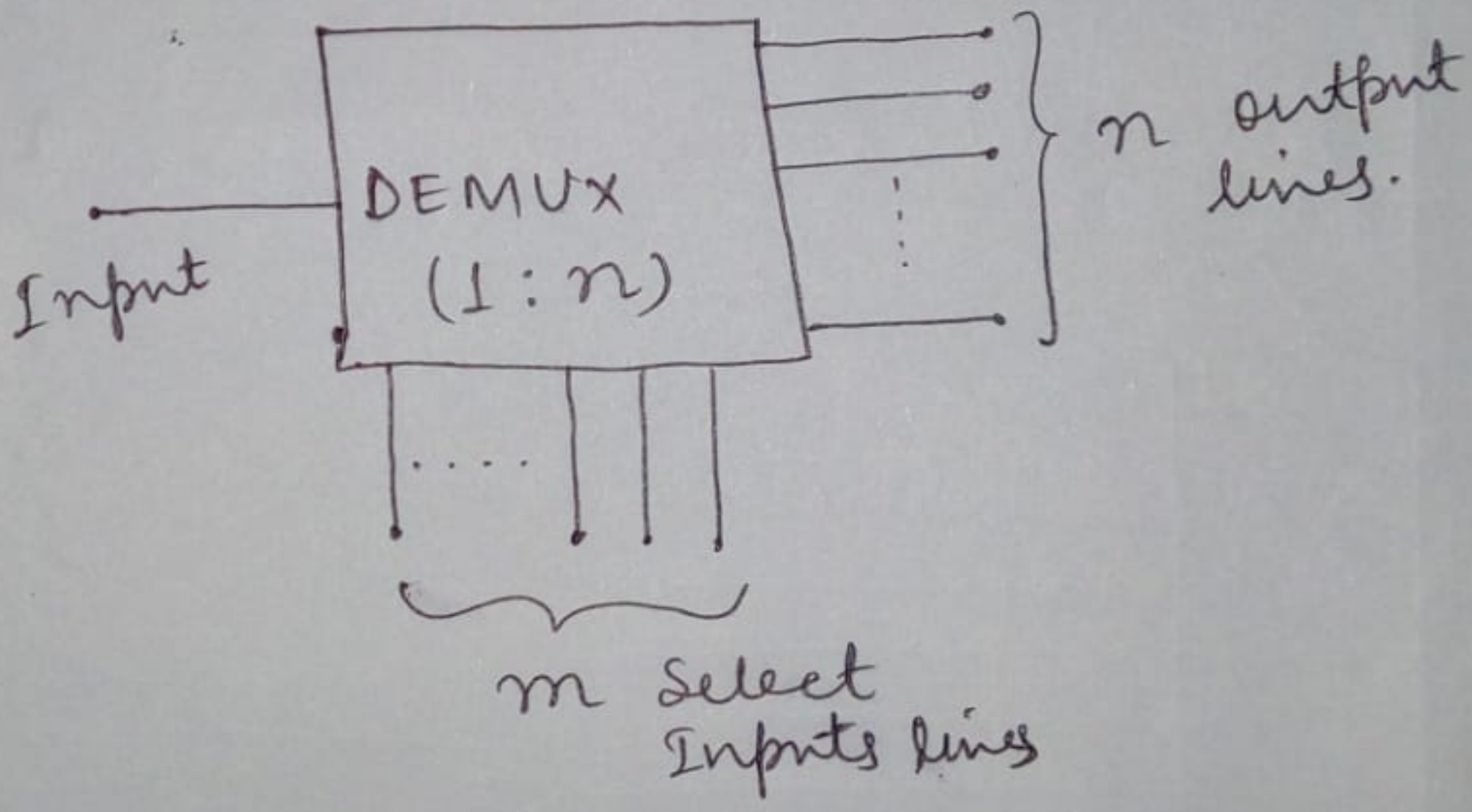
Q.N. 5(b) What is Demultiplexer (DEMUX)? Show with block diagram.

Sol:- **Demultiplexer (DEMUX):-**

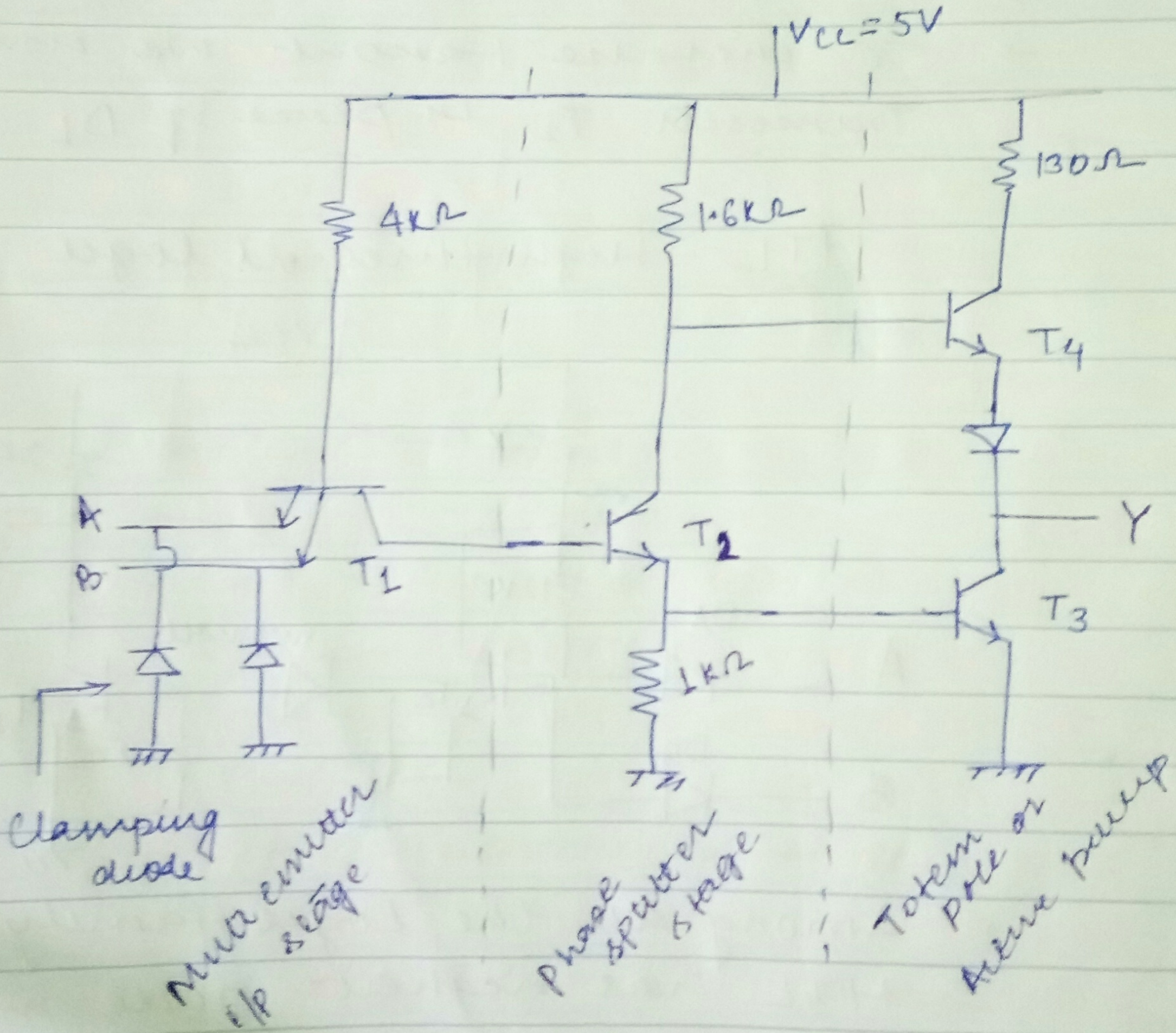
A demultiplexer is combinational logic that receives information on a single input and transmits the same information over one of several ($2^m = n$) output lines.

The output line is selected by m number of select input lines.

Block diagram



6. Solution TTL (Transistor Transistor logic)



TTL basically contains 3-stages.

1. Multi emitter input stage.
2. phase splitter stage
3. Totempole (OR) Active pull up output stage.

A	B	T_1	T_2	T_3	T_4	Y
0	0	Active	cutoff	cutoff	SAT	1
0	1	Active	cutoff	cutoff	SAT	1
1	0	Active	cutoff	cutoff	SAT	1
1	1	Reverse Active	SAT	SAT	CUT	0

TTL operation

→ In TTL logic family, if any of the i/p of logic family is low or all the inputs are low then emitter base junction of T1 is forward biased & collector base junction is reversed biased [T1 is in active mode].

→ Due to this Transistor T_2 & T_3 are cutoff and T_4 is in saturation and output is 1.

→ when all the inputs are high then emitter base junction of T1

is reverse bias and collector base junction is forward bias. Due to this transistor T1 is in reverse active, T_2 and T_3 are in saturation whereas T4 is in cutoff and output is zero.

→ Hence basic gate of TTL is NAND gate.

→ Basic gate - NAND.
→ tpd - 10nsec.
→ Pdiss - 10mwatt
→ F.O.M - 100PJ.
→ Fanout - 10.
→ Noise margin - 0.4 volt.

Advantage of Totem pole conf.

1. Higher speed of operation.
2. Lower power dissipation.
3. Higher fanout.

Disadvantage

→ Not provide wired logic.

To provide wired AND operation, open collector outputs are used in TTL logic family.