Q. N. 1(a)

Ans:- **Diffusion and Drift current**

↳ Diffusion is a process which occurs in the presence of concentration gradient. In this process charge carriers flow from a high concentration region to low concentration region. The flow of charge carriers constitute a current and is called as diffusion current.

In a PN Junction diode, hole concentration is more in p-type semiconductor compared to that in the n-type semiconductor, hence, there exist a hole concentration gradient and due to this holes from p-type semiconductor diffuse towards n-type semiconductor and consitute hole diffusion current. Similarly, there exists an electron diffusion current from p-type semiconductor to n-type semiconductor.

↳ Drift current is the flow of charge carriers caused by the electric field.

↳ The direction of drift current (hole or $\bar{e}$) is always in the direction of electric field, while the direction of diffusion current depends upon the gradient of carrier concentration.

Q.N. 1 (b)

Ans:-

Avalanche Multiplication :-

Avalanche multiplication is a process in a reverse biased PN junction diode, in which thermally generated carriers acquires sufficient energy from the applied reverse bias to disrupt a covalent bond on colliding with a crystal ion. Due to disruption of covalent bond new electron hole pair generated in addition to original carrier. The newly generated carrier may acquire sufficient energy from the applied bias and collide with crystal ion & generate other e-hole pair. This cummulative process of generating new carriers result in a large reverse current in a PN junction diode.

Q.N 2

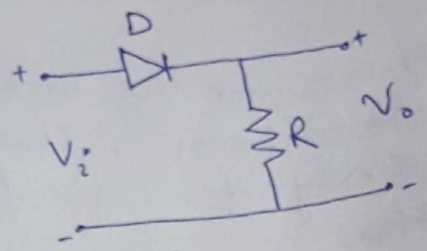
Ans:

Rectification:-

Rectification is a process in which a sinusoidal input waveform (whose average value is zero) is converted into a unidirectional (though not constant) waveform with a non-zero average component.

Half wave Rectifier:-

The circuit diagram of half wave rectifier is shown.



Here,

V_i = Input Sinusoidal Voltage waveform = $V_m \sin \omega t$

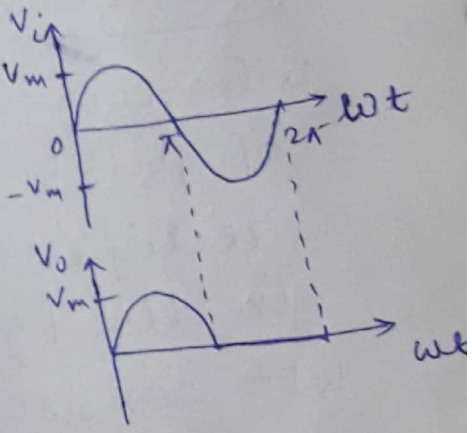
D = Ideal PN junction diode

R = Resistor.

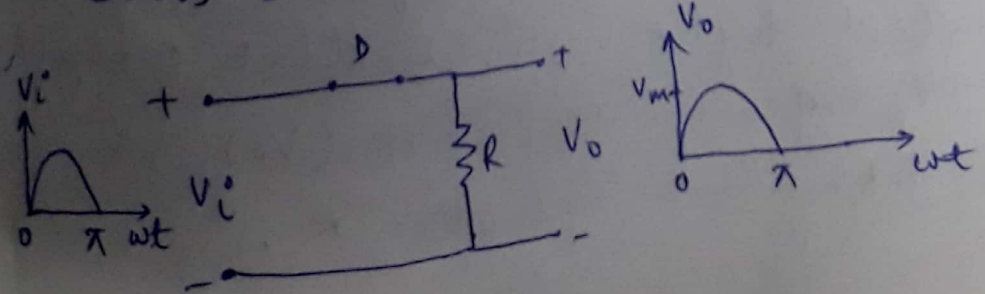
V_o = Output rectified voltage waveform.

working principle:-

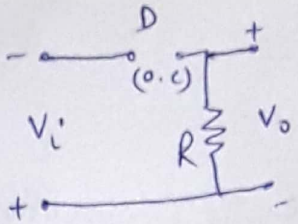
For the positive half cycle of the input waveform (0 to π) the diode (D) is forward biased and acts as short circuited (S.C). Hence, the current will flow through the resistor 'R' and for the entire positive cycle output voltage will appear across the resistor R.

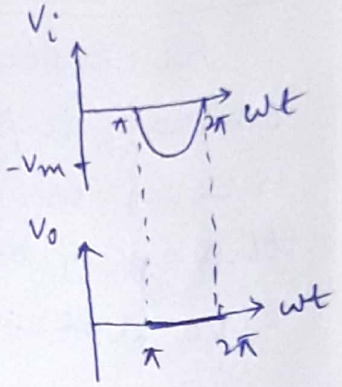


Input and output waveform.



For the negative half cycle diode (D) will be reverse biased and acts as an open circuit (O.C). Therefore, no current will flow through the resistor R and hence output voltage across the resistor R will be zero for the entire negative half cycle.





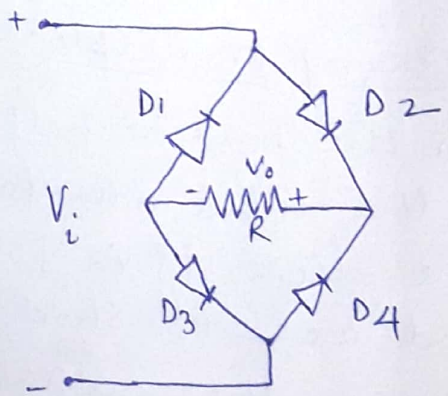
Thus, for the one complete cycle of the input waveform, the output waveform appears only for half cycle (positive cycle).

~~The~~

Full wave Rectifier:-

Bridge Rectifier:-

↳ The circuit diagram of full wave bridge rectifier is shown in the figure.

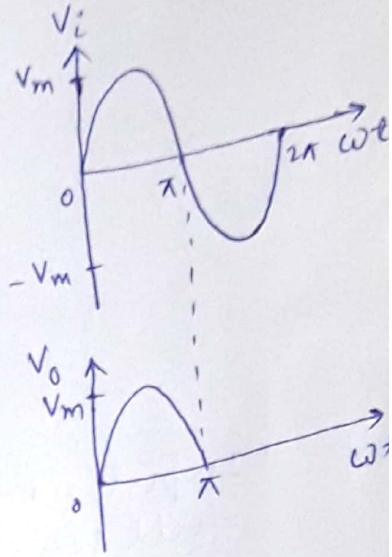


↳ It consist of four diodes (ideal) D_1, D_2, D_3, and D_4 and a resistor R.

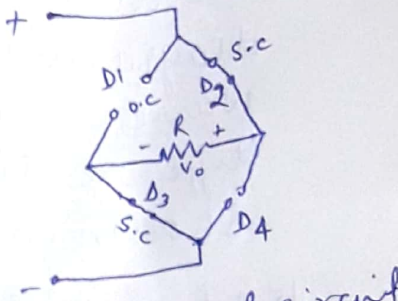
↳ The input sinusoidal voltage waveform is represented by V_i and the output rectified voltage waveform (V_o) is observed across the resistor R.

Working Principle :-

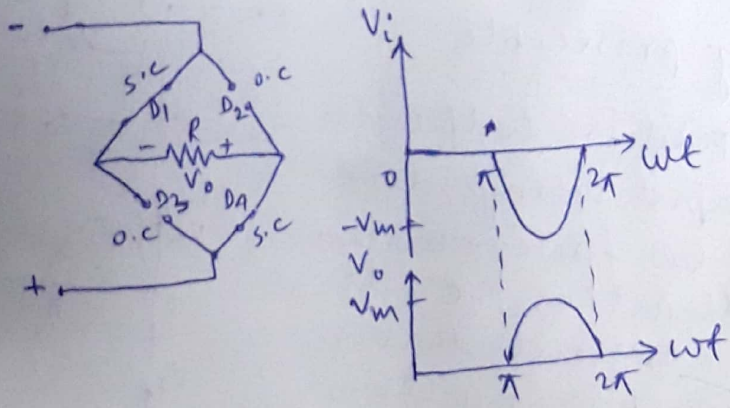
For the positive half cycle of the input voltage (0 to π), ~~the~~ diodes D_2 & D_3 will be forward biased and will act as (S.C). The current will flow through the diode D_2, R, & D_3 and for this half cycle of the input waveform, output voltage will appear across the resistor R.



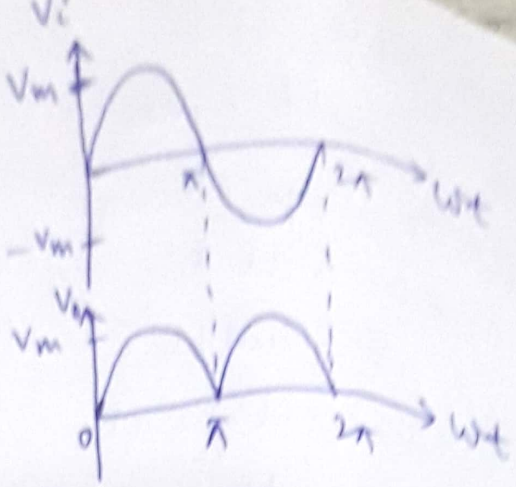
For the negative half cycle of the input waveform (π to 2π), diodes D_1 & D_4 will be forward biased and will act as S.C. The current will flow through the diode D_4, R, and D_1 and for this half cycle the output waveform will ~~act~~ appear across the resistor R.



Equivalent circuit for the Positive Half cycle.



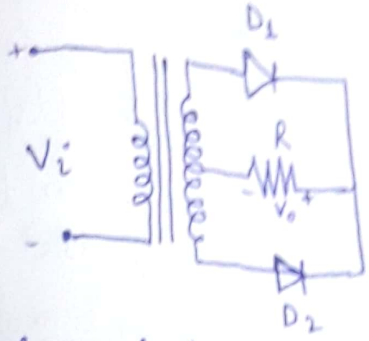
For the entire cycle of the I/p waveform the output waveform is available and the current flows in the same direction through the resist



Input and output waveform of the full wave bridge rectifier circuit.

Center tapped transformer full-wave Rectifier

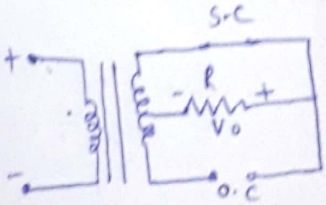
↳ The circuit diagram of full-wave center tape type rectifier is shown in the figure.



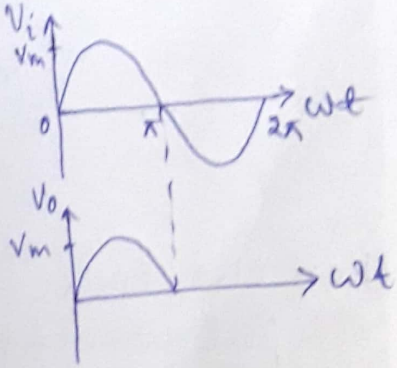
↳ It consists of a center tapped transformer to establish the input signal across each section of the secondary of the transformer

↳ It requires only two diodes (D_1 & D_2) and resistor (R).

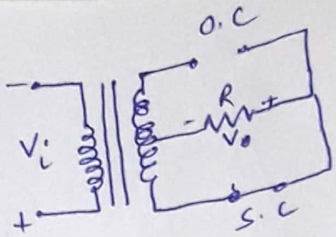
Working principle :-

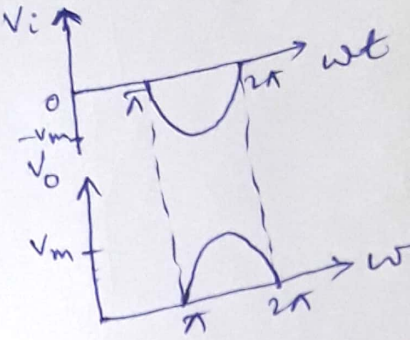


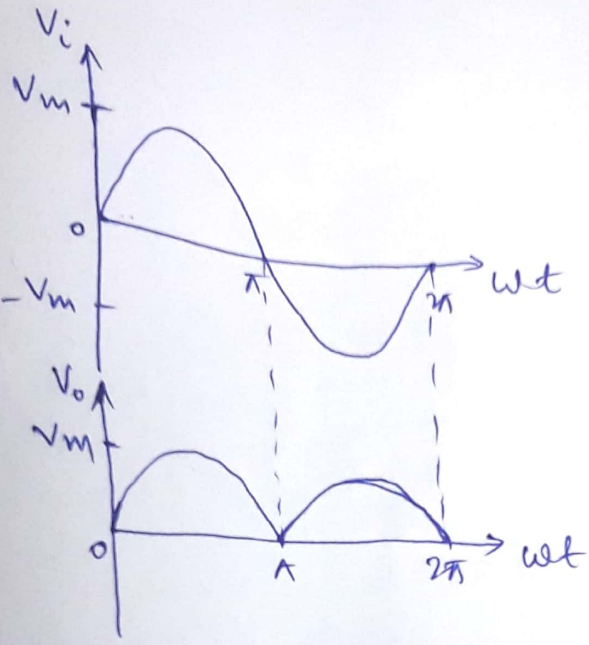
For the positive half cycle of the Input voltage, diode (D_1) will be forward biased and will act as S.C to pass the current through resistor R. During this half cycle output will be appear across the resistor R.



For the negative half cycle the diode (D_2) will be F.B and will act as S.C and allow the current to pass through the resistor R. The output voltage will appear across the resistor for this half cycle also.



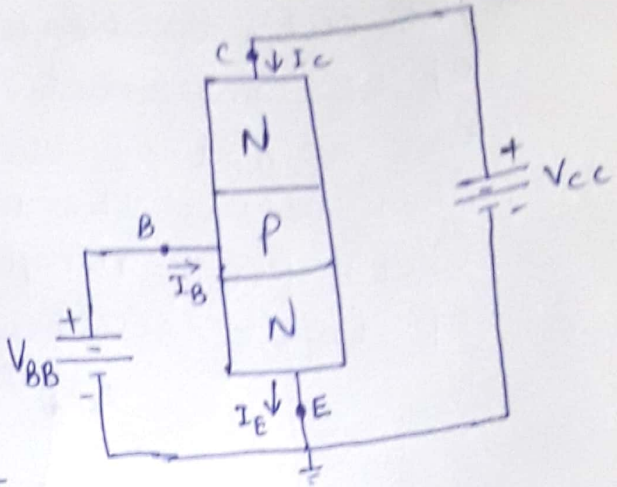




Input and output waveforms of the center tapped type full wave rectifier circuit.

Ans:-

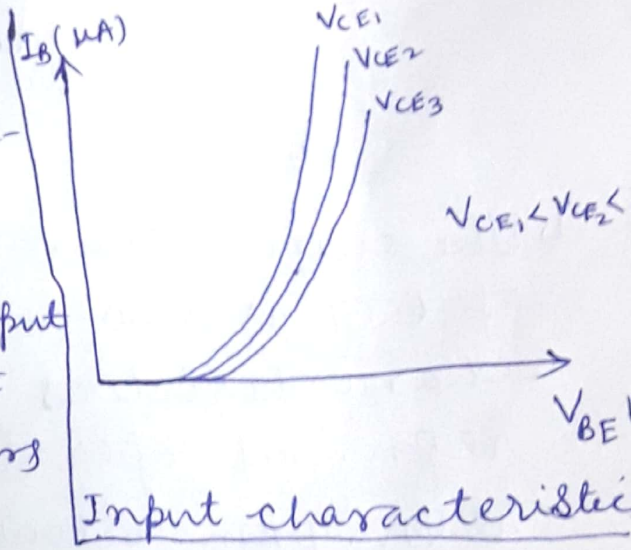
Common Emitter (CE) configuration of BJT



Input characteristics

↳ Input characteristics of CE-configuration of BJT is a plot of input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

↳ For the CE-configuration of BJT, the input characteristics is shown in the figure.

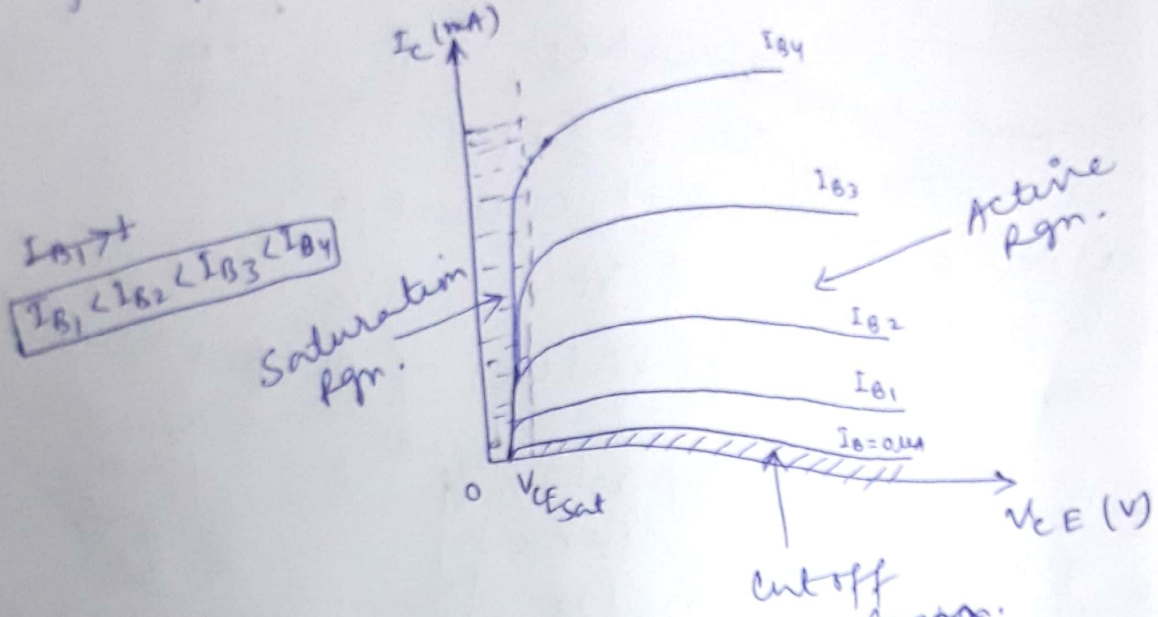


↳ For a fixed value of output voltage (V_{CE}) the input characteristic appears as the V-I characteristic of PN junction diode.

↳ With the increase in the output voltage (V_{CE}) the characteristic shift to the right.

Output characteristics

↳ The output characteristics of CE-configuration of BJT are a plot of output current (I_C) versus the output voltage (V_{CE}) for a range of values of input current (I_B).



↳ The output characteristic of CE-config. of BJT is shown above. The output characteristics have three different regn. of operation namely- cutoff regn. (Rgn. below $I_B < 0\mu A$), Saturation rgn. (Rgn. left to the $V_{CE} = V_{CEsat}$, i.e $V_{CE} < V_{CEsat}$) and Active rgn. (Rgn. $I_B > 0\mu A$ & $V_{CE} > V_{CEsat}$). With the increase in input current (I_B) the output current (I_C) increases.

Q. (4)

(a) Explain thermal runaway in Transistor.

Def:- The max^{m} average power $P_{D,max}$ which a transistor can dissipate depends upon the transistor construction and may lie in the range from few milli-watts to 200W. The maximum power is limited by the temperature that the Collector-to-Base Junction can withstand. The Junction temp. may rise either because the ambient temp. rises or due to self-heating. As a consequence of Junction Power dissipation, the Junction temperature rises, and this in turn increases the collector current, with a subsequent increase in power dissipation. If this phenomenon continues Thermal runaway takes place.

b) State the application of LED.

P
1. used in Lighting & illumination.
2. used in mining operations, as cap lamps.
3. LED is used for transmit data & analog signals.
4. LED used in optical fiber equipments.
5. LED used in medical field.

Q-5 Explain the construction and working of N-channel [illegible].

(c) Explain Intrinsic & Extrinsic semiconductor.

Sol^n Intrinsic semiconductor → An intrinsic semiconductor is one which is made of the semiconductor material in its extremely pure form. Ex- Si, Ge, GaAs

Extrinsic semiconductor :- → A semiconductor material that has been subjected to the doping process is called an Extrinsic material.

There are two types of Extrinsic semiconductor material :—

(a) N-Type

→ If doping is done with pentavalent impurity, N-type semiconductor forms.

Pentavalent impurity :— As, P, Sb..

(b) P- Type

→ If doping is done with Trivalent impurity, P-type semiconductor forms.

Trivalent impurity :— B, Ga, In ...

—x—

Q-5 Explain the construction and working of N-channel JFET with suitable diagram.

The JFET is a three-terminal unipolar device with one terminal capable of controlling the current between the other two terminal

JFET is of two types → N-channel JFET
→ P-channel JFET

Constructional Details of N-channel JFET

N-JFET has lightly doped N-region sandwiched between two P-type regions as shown in fig. below. The middle N-region is the channel of JFET and P-regions form the Gates. A JFET with n-type channel is called N-channel JFET.

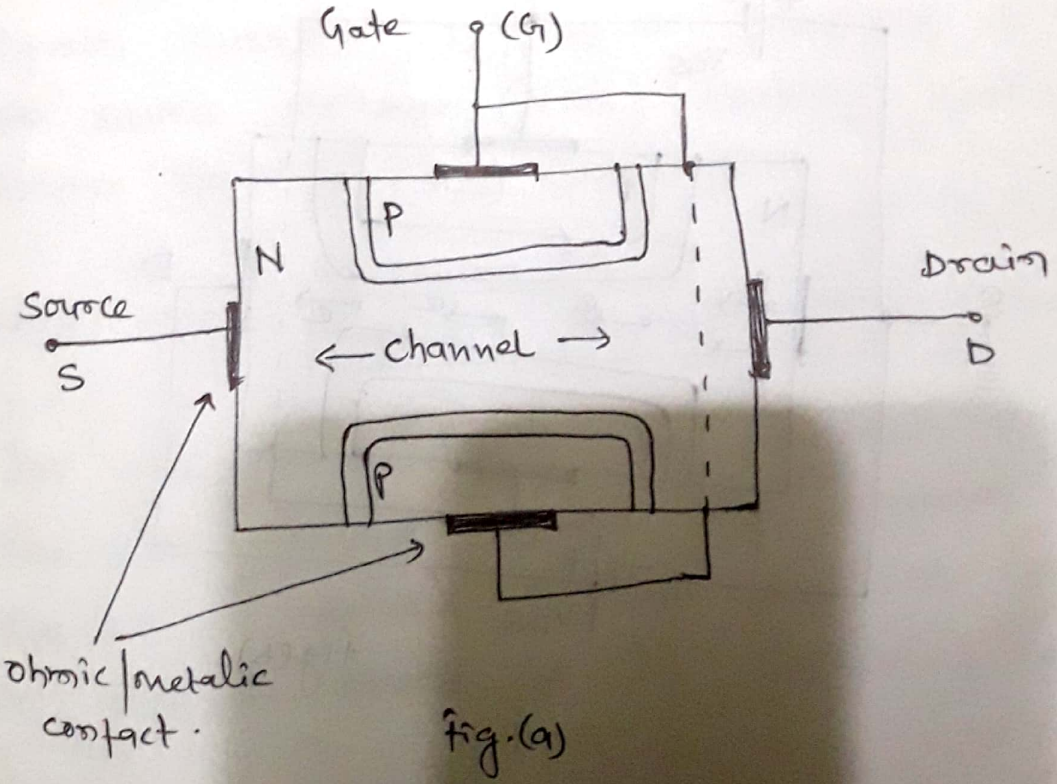


fig.(a)

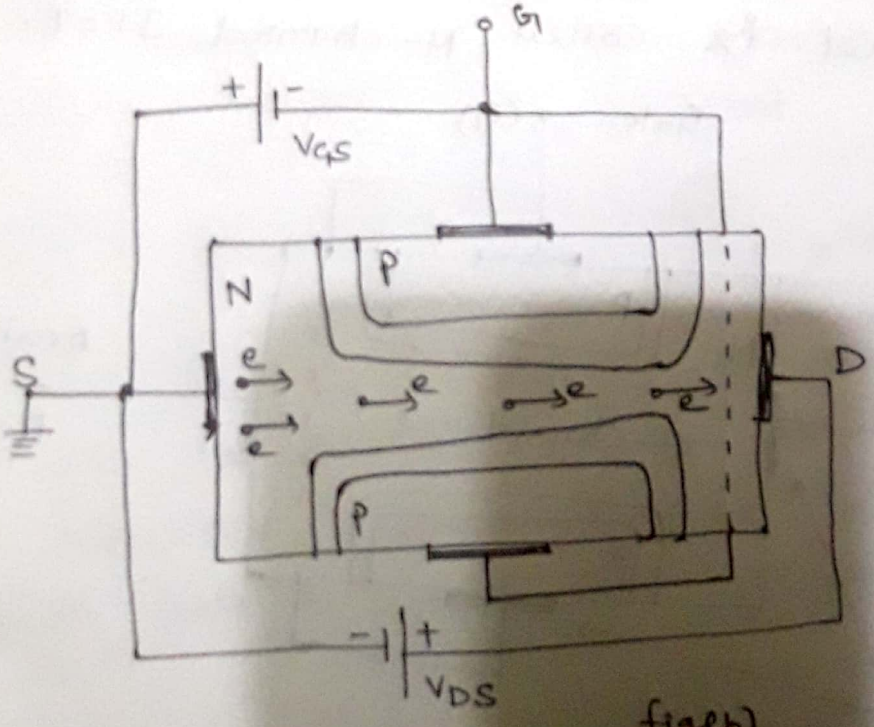
The three terminals of N-JFET is biased such as r.t. in voltage is reverse.

N-JFET has three terminals —

(a) Gate
(b) Source
(c) Drain

One end of the channel is designated as source and the other end as Drain. Usually the source & Drain are interchangeable. For N-JFET, the terminal to which higher potential is applied acts as the Drain. the drain terminal collects the charge carriers emitted from the source through the channel. the Gate terminal controls the flow of current through the channel.

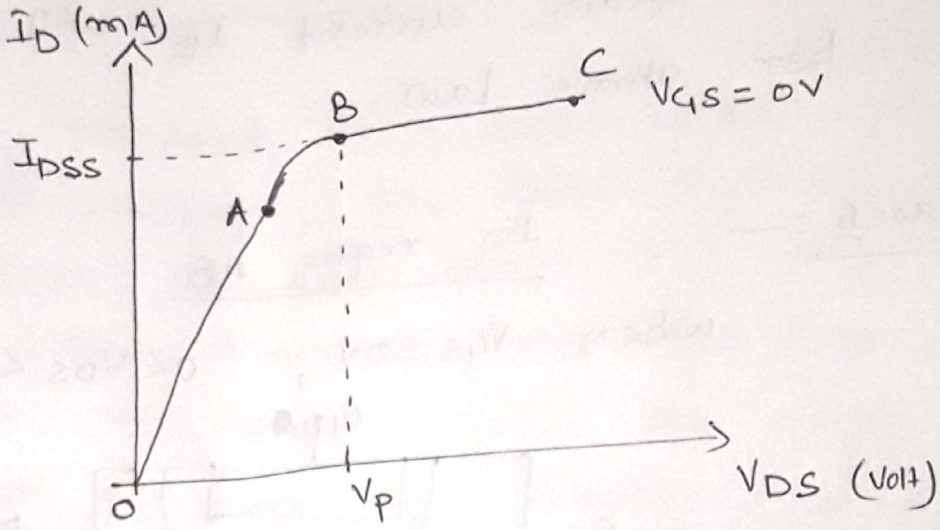
→ Working principle :→



fig(b)

The three terminals of N-JFET is biased such as Gate to source voltage is reverse biased and Drain terminal is at positive potential compare to source terminal.

Drain characteristics



The working of N-channel JFET will best explain with Drain characteristics. The Drain characteristics of JFET is plot of Drain current (I_D) as a function of Drain to source voltage (V_{DS}) keeping Gate to source voltage (V_{GS}) constant.

Case1 when **In region OA**
$V_{GS} = 0V$ & V_{DS} = some positive value.

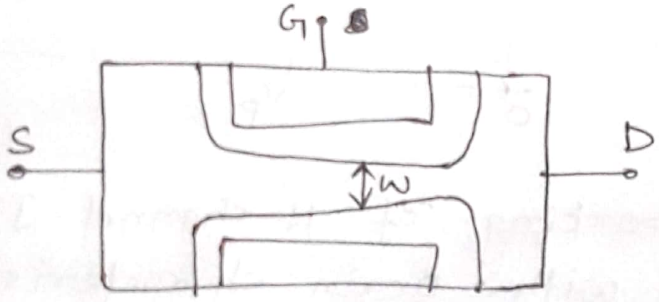
In the given fig(b), a positive voltage V_{DS} is applied across the channel and $V_{GS} = 0V$ applied across Gate-source terminal. So Gate to source is in unbiased condition.

C When the voltage $V_{DS} > 0$ is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D. The drain current I_D depends on resistance offer by N-channel.

* When V_{DS} is increases from 0V to few vo the drain current I_D will increase as per ohm's law.

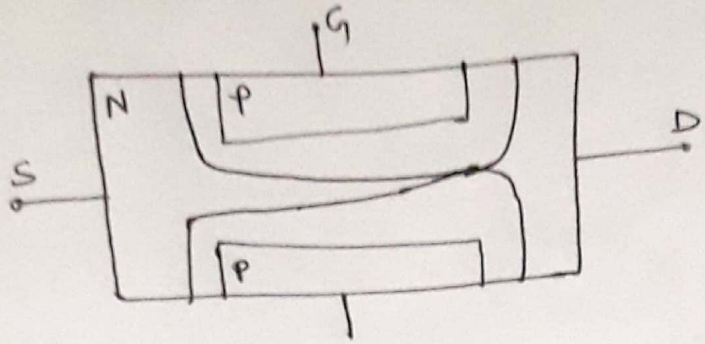
Case I :— In region AB.

when $V_{GS} = 0V$, $0 < V_{DS} < V_P$ (Pinch-off voltage)



As the V_{DS} increases and approches to Pinch-off voltage (V_P), the depletion region will widen, causing a noticeable reduction in the channel width. The reduce path of conduction causes the resistance to increase and the variation of current in this region becomes curvilal.

Case III :→ $V_{GS} = 0V$ & $V_{DS} \geq V_p$ (In region BC)



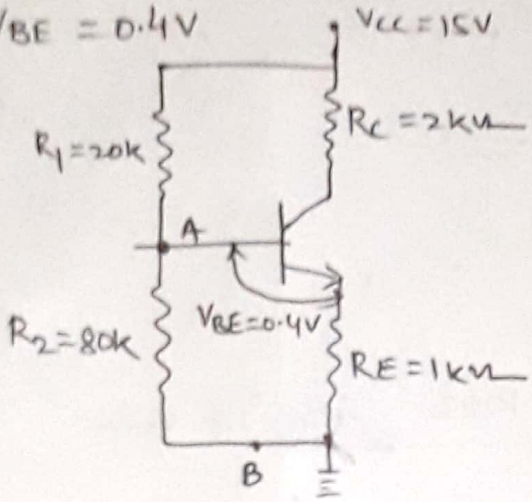
If the V_{DS} is increased to a level where $V_{DS} > V_p$ (Pinch-off voltage), the two depletion region will touch to each other and this condition is called Pinch-off. In this case in reality a very small channel still exists, with a current of very high density. This is the fact that I_D doesn't drop off at Pinch-off and maintain the saturation level (I_{DSS}.)

→ when $V_{GS} < 0$ (Gate-Source terminal is reverse Biased)

The Pinch-off voltage V_p of JFET is smaller in this case compare to $V_{GS} = 0$ condition. So that Saturation current (I_{DSS}) becomes Smaller compare to unbiased case.

Q. (6) Find the value of I_B & I_C in the given circuit.

Given, $\beta = 100$, $V_{BE} = 0.4V$



Soln

Apply Thevenin theorem in I/p side of voltage divider ckt —

Calculation of R_{Th} — Thevenin Resistance

V_{Th} — Thevenin voltage

For R_{Th}. (Across AB)

Put $V_{cc} = 0V$.

So, $R_{Th} = R_1 \| R_2 = \frac{20 \times 80}{20+80} = 16 k\Omega$

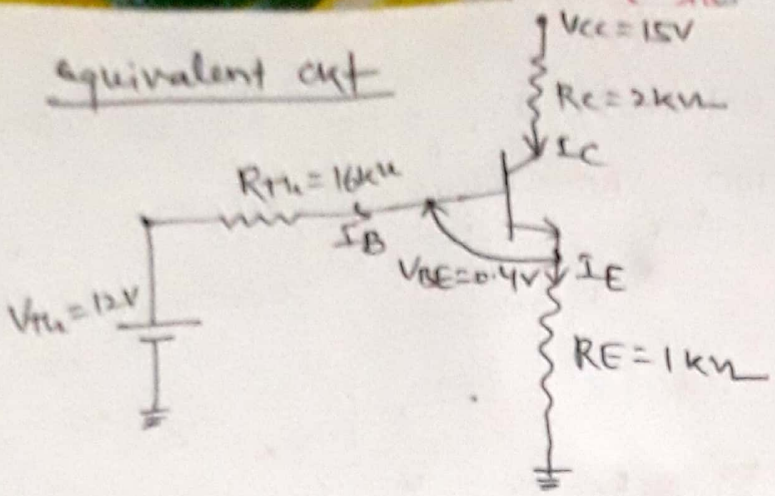
$\boxed{R_{Th} = 16k\Omega}$

V_{Th} = voltage across R_2

$= \frac{R_2}{R_1+R_2} V_{cc} = \frac{80}{20+80} \times 15\ V = 12V.$

$\boxed{V_{Th} = 12V.}$

Equivalent ckt



Applying KVL in i/p side.

$$V_{Th} = R_{Th} \cdot I_B + V_{BE} + R_E \cdot I_E$$

$$V_{Th} = R_{Th} I_B + V_{BE} + R_E \cdot \beta I_B$$

$$\Rightarrow V_{Th} - V_{BE} = (R_{Th} + \beta R_E) I_B$$

$$\therefore I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + \beta R_E}$$

$$= \frac{12 - 0.4}{(16 + 100 \times 1)\,k\Omega} = \frac{11.6}{116\,k\Omega} = \frac{1}{10}\,mA$$

$$\boxed{I_B = 0.1\,mA}$$

As. $I_E \simeq I_C$

$I_E = \beta I_B$

$$I_C = \beta I_B$$

$$= 100 \times 0.1\,mA$$

$$= 10\,mA$$

$$\boxed{I_C = 10\,mA}$$

→ The value of I_C is very high. So theoritically it is possible but practically not possible.