(1) **Two Transistor model of a Thyristor:-**

The principal of thyristor operation can be explained with the use of two transistor model or two transistor analogy. Two transistor model is obtained by bisecting the middle layers along the dotted line, in two seperate halves as shown in figure. In this figure junctions J_1-J_2 and J_2-J_3 can be considered to constitute pnp & npn transistors separately. The circuit representation of the two transistor model of a thyristor is shown in figure.

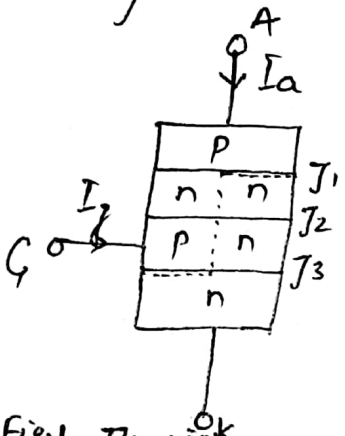


Fig.1. Thyristor.

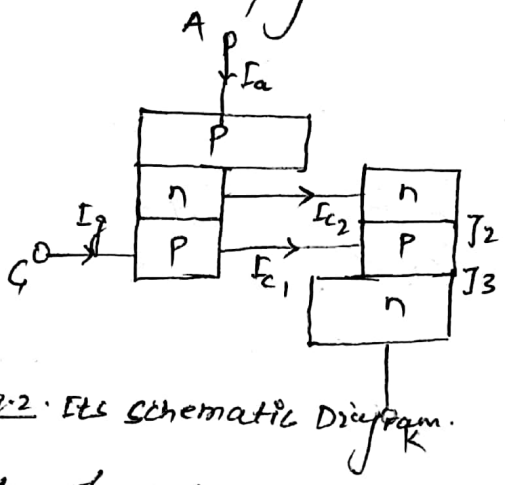


Fig.2. Its Schematic Diagram.

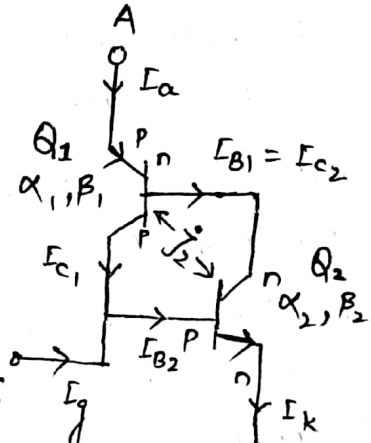


Fig.3. Its Two-Transistor model.

In the off state of a transistor, collector current I_c is related to emitter current I_E as,

$$I_c = \alpha I_E + I_{CBO},$$

where α is the common base current gain and I_{CBO} is the common base leakage current of collector base junction of a transistor.

For transistor Q_1 in fig 3. emitter current I_E = anode current I_a and I_c = collector current I_{c1}. Therefore for Q_1,

$$I_{c1} = \alpha_1 I_a + I_{CBO1}, \quad \text{where, } \alpha_1 = \text{common-base current gain of } Q_1.$$

— (I) $\quad I_{CBO1} = \text{common-Base leakage current of } Q_1.$

Similarly for transistor Q_2, the collector current I_{c2} is given by,

$$I_{c2} = \alpha_2 I_k + I_{CBO2}, \quad \text{where, } \alpha_2 = \text{common-base current gain of } Q_2.$$

— (II) $\quad I_{CBO_2} = \text{common-Base leakage current of } Q_2.$

I_k = Emitter current of Q_2.

The sum of two collector currents given by equations (I) & (II) is equal to external circuit current I_a entering at anode terminal A.

$$\therefore I_a = I_{c1} + I_{c2}$$

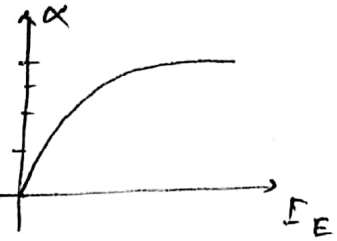
$$= \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \quad \text{— (III)}$$

When Gate current is applied, then $I_k = I_a + I_g$. substituting this value of I_k in eqn (III) gives,

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

$$I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)} \quad \text{(IV)}$$

For a silicon transistor, current gain α is very low at low emitter current. With an increase in emitter current, α builds up rapidly as shown in figure below.

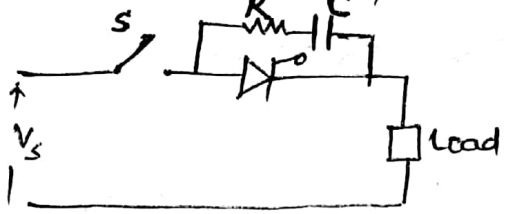


With Gate current $I_g = 0$, and with thyristor f.biased, $(\alpha + \alpha_2)$ is very low and forward leakage current somewhat more than $(I_{CBO1} + I_{CBO2})$ flows. If by some means, the emitter current of two component transistors can be increased so that $\alpha_1 + \alpha_2$ approaches unity then I_a would tend to become infinity thereby turning 'on' the device.

(2) Snubber circuit & Its operation.

If the rate of rise of forward voltage $\frac{dv_a}{dt}$ is high, the charging current will be more. This charging current plays the role of gate current and turns on the SCR even when gate signal is zero. Such phenomena of turning on thyristor must be avoided as it leads to false operation of thyristor circuit.

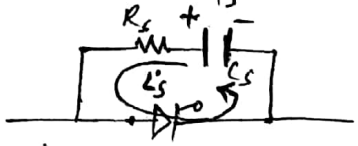
To protect the SCR from high $\frac{dv_a}{dt}$, snubber circuit is used. It consists of a capacitor in series with a current limiting resistor & this combination is connected across the thyristor which is to be protected.



Operation:-

When switch S is closed, a sudden voltage appears across the ckt. capacitor behaves like short circuit, therefore voltage across SCR is zero. With the passage of time voltage across C_s builds up at a slow rate such that $\frac{dv}{dt}$ across C_s and therefore across SCR is less than the specified max^m $\frac{dv}{dt}$ rating of the device.

Before SCR is fired by gate pulse C_s charged to full voltage V_s. When C_s discharges through the SCR and sends a very high current as the resistance of loop is very low. to limit this current a resistance R_s is connected is series.



$i_s \uparrow\uparrow$ if $R_s = 0$.

* For AC supply, when sudden noise comes in supply voltage of very high frequency, then it affects the $\frac{dv}{dt}$ value as $\frac{dv}{dt} \propto \omega$.

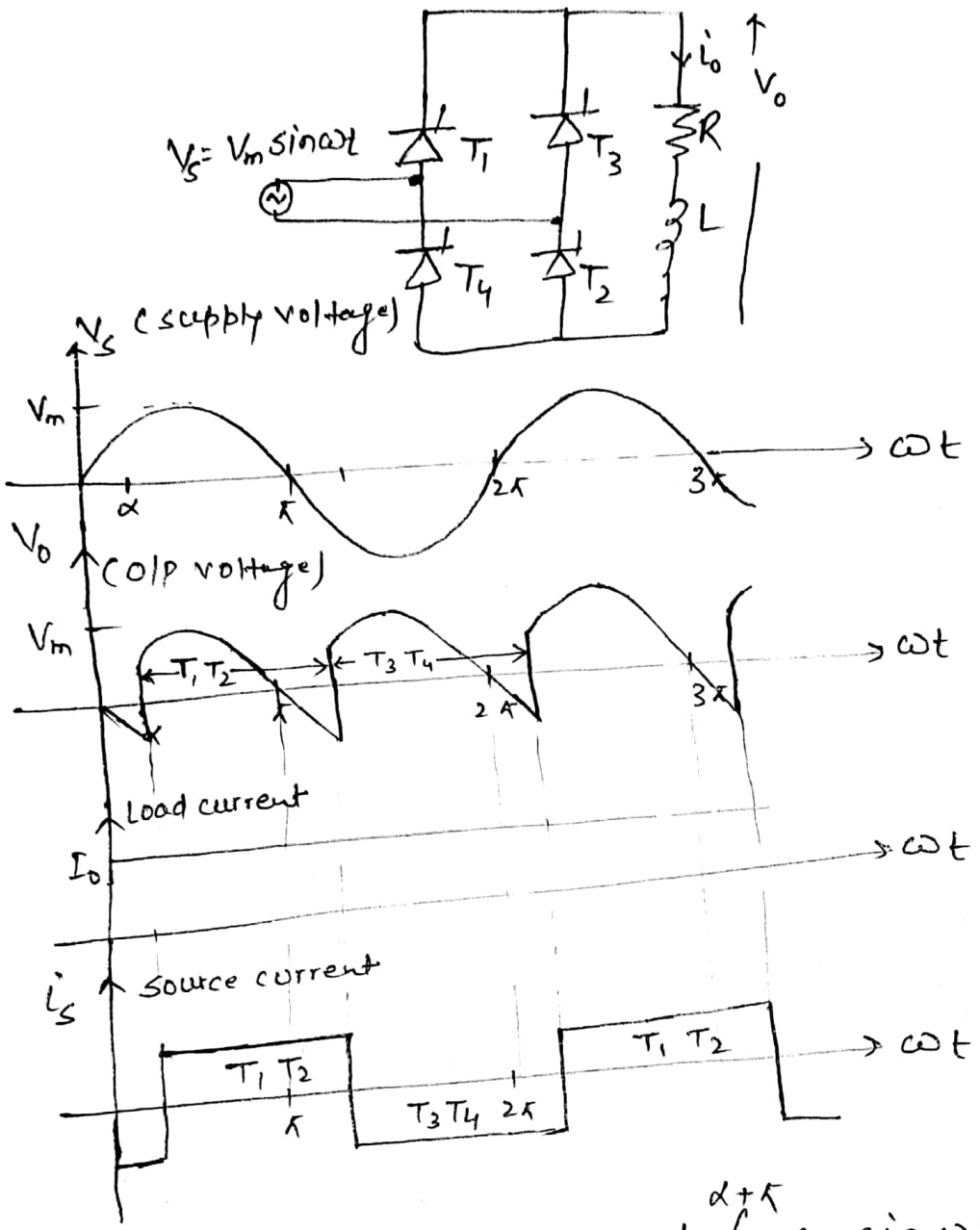
let $V_a = V_m \sin\omega t$

$$\frac{dv_a}{dt} = V_m \cdot \omega \cdot \cos\omega t \Rightarrow \boxed{\frac{dv_a}{dt} \propto \omega.}$$

This sudden increase in frequency due to noise signal, increased $\frac{dv}{dt}$ & hence the anode current. & If this anode current surpass the latching current it leads to false turn on of thyristor.

As the freq. increases impedance $\left(\frac{1}{\omega C}\right)$ of capacitance decreases bypass the current & hence thyristor gets protected.

(3.) Single phase full-wave Rectifier with R-L Load :-



Average output voltage $V_{OAvg} = \frac{1}{\pi} \int_{\alpha}^{\alpha+\pi} V_m \sin\omega t \, d\omega t$

$\therefore V_{OAvg} = \frac{1}{\pi} \cdot V_m (-\cos\omega t)_{\alpha}^{\alpha+\pi}$

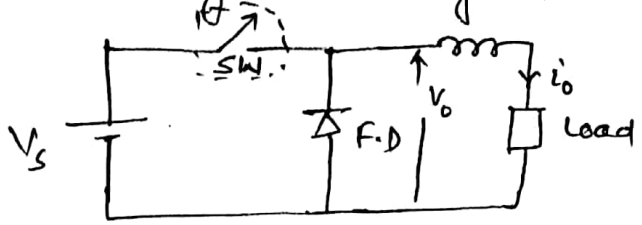
$= \frac{V_m}{\pi} (-\cos(\pi+\alpha) + \cos\alpha) = \frac{V_m}{\pi} \cdot (2\cos\alpha)$

$V_{OAvg} = \frac{V_m}{\pi} (2\cos\alpha)$

$$\boxed{V_{OAvg} = \frac{2V_m}{\pi} \cos\alpha}$$

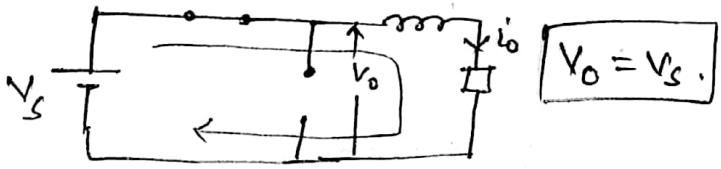
(4.) Step-down Chopper:-

Step-down chopper converts high DC-voltage to low dc-voltage.



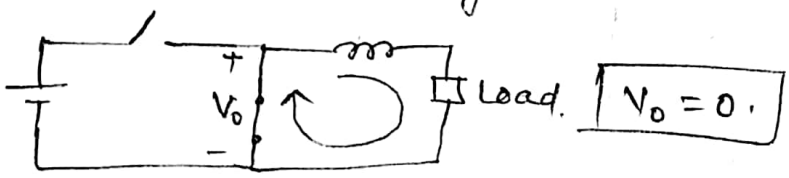
Case-I: When switch SW is closed.

In this case the voltage across the F.D is V_s & thus it is reverse biased. hence the o/p voltage V_o is equal to the supply voltage (V_s) & the current passes through the supply voltage to inductor to Load.

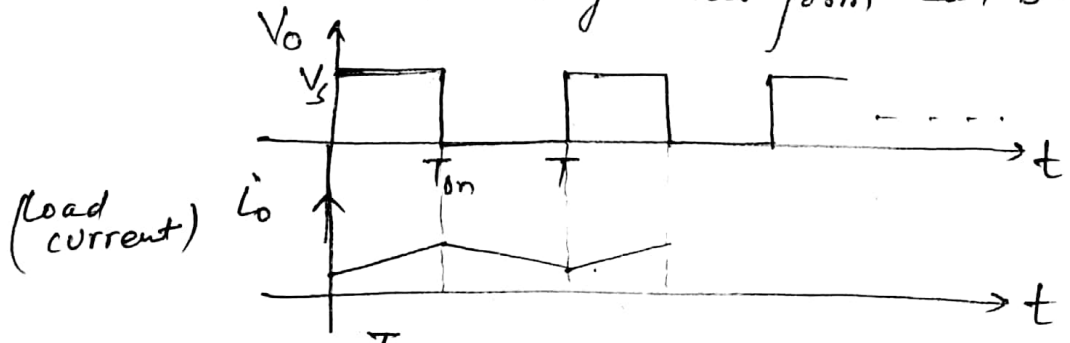


Case-II: When switch SW is Open:-

In this case inductor discharges through load, & current passes through freewheeling diode. Since freewheeling diode is in on-state, voltage V_o becomes zero.



From these two cases o/p voltage waveform can be drawn as.



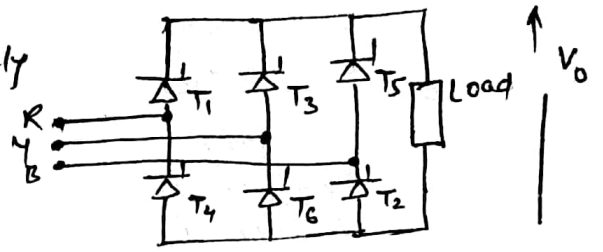
$$V_{oAvg} = \frac{1}{T}\int_0^{T_{on}} V_s \cdot dt = \frac{1}{T} \cdot V_s \cdot (t)_0^{T_{on}}$$

$$= V_s \cdot \frac{T_{on}}{T}$$

$\therefore$ $\boxed{V_{oAvg} = V_s \cdot \delta}$ Where δ = duty ratio.

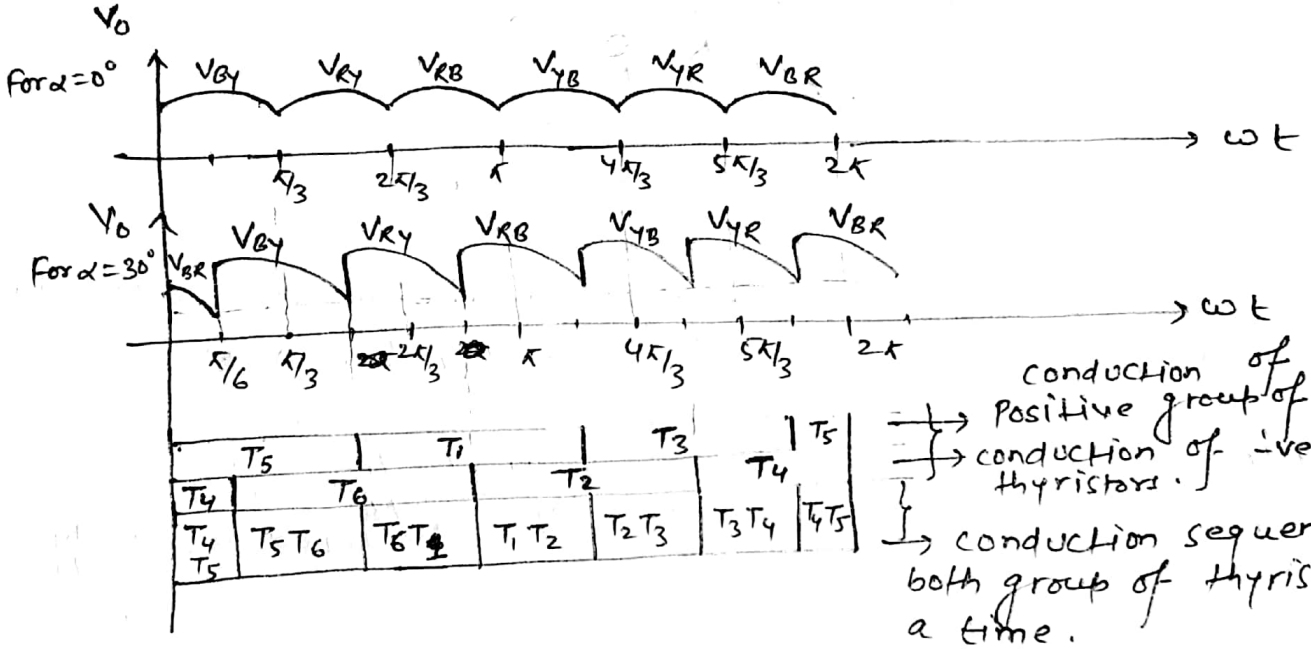
(2.5) 3-Phase Full-wave Rectifier:-

3-ϕ full wave converter is a fully controlled bridge controlled rectifier using six thyristors connected in form of a full wave bridge configurations.



All the six thyristors are controlled switches which are turned on at a appropriate times by applying suitable gate trigger signals.

The thyristors are triggered at interval of 60°.



→ conduction of Positive group of thyristor
→ conduction of -ve group of thyristors.
→ conduction sequence of both group of thyristor at a time.

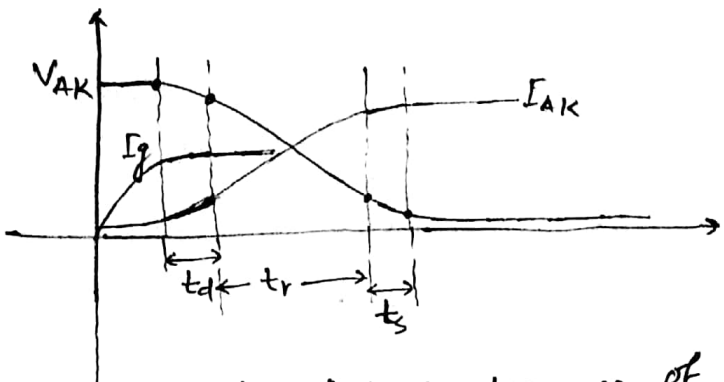
From the above output voltage waveform it is clear that the ~~o/p voltage~~ converter will be in continuous mode for $\alpha \leq 60°$.
& hence, for $\alpha \leq 60°$,

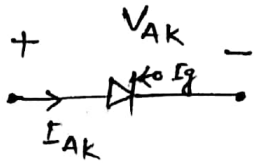
$$V_{0Avg} = \frac{1}{\pi/3} \int_{30°+\alpha}^{60°+\alpha} V_{mL} \sin(\omega t + 30°)\, d\omega t$$

$$= \frac{1}{\pi/3} \cdot V_{mL} \cos\alpha = \frac{3V_{mL}}{\pi} \cos\alpha.$$

$$\therefore \boxed{V_{0Avg} = \frac{3V_{mL}}{\pi} \cos\alpha}$$

Q.6. Turn-on characteristics of SCR:-





As we initiates turning on process of a thyristor by giving appropriate gate signal, the voltage across the thyristor starts decreasing and current (anode current) starts increasing. When thyristors becomes fully conductional, the anode to cathode voltage (V_{AK}) becomes the on-state voltage drop (1v-2v) and the anode current rated value.

Turn on time of thyristor can be devided in to 3- catagories.

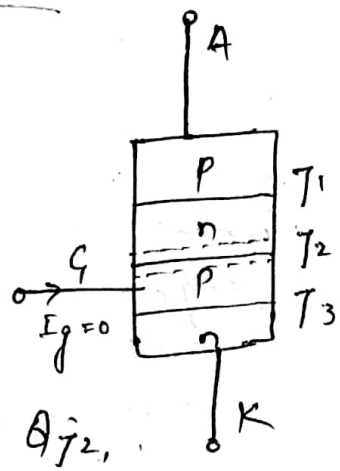
i) Delay time (t_d) It depends on the gate signal amplitude. It is the time in which V_{AK} changes from V_{AK} to $.9\,V_{AK}$, current (I_A) from leakage current from $.1\,I_{AK}$ or gate current from $.9\,I_g$ to I_g.

ii) Rise time (t_r):- It depends on the load parameters. It is the time in which V_{AK} changes from $.9\,V_{AK}$ to $.1\,V_{AK}$ & anode current from $.1\,I_A$ to $.9\,I_A$.

iii) Spread time (t_d) :- During spread time, the current density spreads throughout cross sectional area of SCR, therefore spread time depends on the physical geometrical structure of the device.

It is the time in which V_{AK} changes from $.1\,V_{AK}$ to on-state voltage drop & anode current (I_A) from $.9\,I_A$ to I_A.

* $\frac{dv}{dt}$ triggering of thyristor:-



In forward blocking mode, at junction J_2, there is a capacitor formed.

let the junction J_2 has a capacitance of C_{J_2} and has a charge accumulated on it is Q_{J_2}.

So, we can write,

$$Q_{J_2} = C_{J_2} \cdot V_{AK} \quad \text{——} (1)$$

Differentiating this eqn. w.r.t. time.

$$\frac{dQ_{J_2}}{dt} = C_{J_2} \cdot \frac{dv_{AK}}{dt}$$

$$i_A = C_{J_2} \cdot \frac{dv_{AK}}{dt}$$

$$\boxed{i_A \propto \frac{dv_{AK}}{dt}}.$$

Since $i_A \propto \frac{dv_A}{dt}$, As $\frac{dv_A}{dt}$ increases i_A also increases. & if this increase in i_A becomes greater than the latching current thyristor will be turn on without any gate pulse.