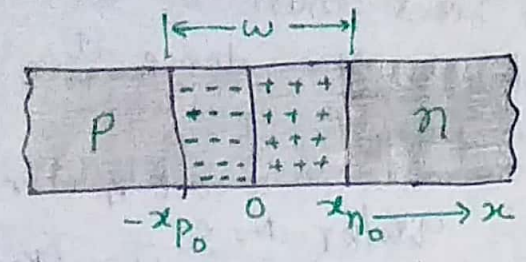
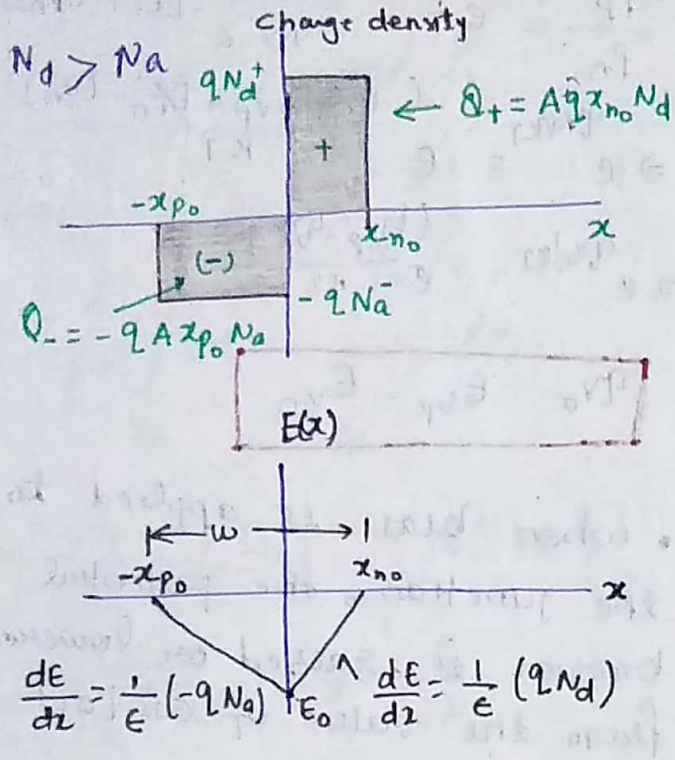
Space charge at a junction.





- With no transistion region, electrons and holes are in transit from one side of the junctia to other side.
- some electrons diffuse from n to p and some are swept by the electric field from p to n. (same as holes).
- Negeleting carriers with in the space charge region, the charge density on the p side is $-qN_a$ and chape density on n side is $+qN_d$.
- The assumption of carrier depletion with in W and neutrality outside W is known as depletion approximation.
- The dipole about the junction must have an equal number of charges on either side ($Q^+ = Q^-$).
- The transistion region may extend into the p and n region unequally, depending upon relative doping of the two sides.
- The total uncompensated charge on either side of the junction

$$Q_+ = Q_-$$

$$\Rightarrow qAx_{n_0}N_d = qAx_{p_0}N_a.$$

A = Area of cross-section

x_{n_0} = penetration of space charge region into the n-material

x_{p_0} = penetration of space charge region into p material.

- To calculate electric field distribution. the poisson's equation

$$\frac{dE(x)}{dx} = \frac{\rho}{\epsilon}(P - N + N_d^+ - N_a^-)$$

poission equation – The gradient

of electric field to the local space charge at any point x

$$\frac{dE(x)}{dx} = \frac{q}{\epsilon}\left(p - n + N_d^+ - N_a^-\right)$$

- $\frac{dE(x)}{dx} = \frac{q}{\epsilon} N_d \quad 0 < x < x_{n_0}$

$$\frac{dE(x)}{dx} = \frac{q}{\epsilon}\left(-N_a^-\right) = -\frac{q}{\epsilon} N_a^-$$

$-x_{p_0} < x < 0$.

- E(x) Vs x, within the transition region has two slopes, positive on the n side and negative on the p side
- There is maximum value of field E_0 at x=0 (Junction between the p and n materials) and E(x) is everywhere negative within depletion region.
- we know that electric field actually points in −x direction from n to P.
- The electric field is assumed to go to zero at the edges of the transition region
- maximum E_0 at the junction since this point is between the +Q and −Q on the either side of the transition region.
- All the electric flux is passes through the x=0 plane, so this is obvious point of maximum electric field.

now

$$\int_{E_0}^{0} dE = \frac{q}{\epsilon} N_d \int_0^{x_{n_0}} dx \qquad (0 < x < x_{n_0})$$

$$\Rightarrow (0 - E_0) = \frac{q}{\epsilon} N_d x_{n_0}$$

$$\Rightarrow E_0 = -\frac{q}{\epsilon} N_d x_{n_0}$$

Similarly.

$$\int_0^{E_0} dE = -\frac{q}{\epsilon} N_a \int_{-x_{p_0}}^{0} dx$$

$$\Rightarrow E_0 = -\frac{q}{\epsilon_0} N_a (x_{p_0})$$

$$E_0 = -\frac{q}{\epsilon} N_a x_{p_0}$$

Therefore maximum electric field $E_0 = -\frac{q}{\epsilon} N_a x_{p_0} = +\frac{q}{\epsilon_0} N_d x_{n_0}$

Now, electric field at any x is the negative of the potential gradient at that point.

$$E(x) = -\frac{dV(x)}{dx}$$

$$\Rightarrow -V_0 = \int_{-x_{p_0}}^{x_{n_0}} E(x)\,dx$$

- Negative of the contact potential is simply area under the $E(x)$ Vs x curve.

$$V_0 = -\frac{1}{2} E_0 W = \frac{1}{2}\frac{q}{\epsilon} N_d x_{n_0} W$$

Since balance of charge requires

$$x_{n_0} N_d = x_{p_0} N_a \quad - (1)$$

$$W = x_{n_0} + x_{p_0}$$

$$\Rightarrow x_{n_0} N_d = (W - x_{n_0}) N_a$$

$$\Rightarrow x_{n_0} N_d = W N_a - N_a x_{n_0}$$

$$\Rightarrow x_{n_0}(N_a + N_d) = W N_a$$

$$\Rightarrow x_{n_0} = \frac{W N_a}{N_a + N_d}$$

Now,

$$V_0 = \frac{1}{2}\frac{q}{\epsilon} N_d \frac{W^2 N_a}{N_a + N_d}$$

$$\Rightarrow W = \left[\frac{2\epsilon V_0}{q}\left(\frac{N_a + N_d}{N_d N_a}\right)\right]^{1/2}$$

$$\boxed{W = \left[\frac{2\epsilon V_0}{q}\left(\frac{1}{N_d} + \frac{1}{N_a}\right)\right]^{1/2}}$$

- $W = \left[\frac{2\epsilon KT}{q^2} \ln\left(\frac{N_a N_d}{n_i^2}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]^{1/2}$

- We can calculate the penetration of the transistion region into the n and p materials

$$x_{p_0} = \frac{W N_d}{N_a + N_d}$$

$$x_{p_0} = \left[\frac{2\epsilon V_0}{q}\frac{(N_a + N_d)}{(N_d N_a)}\right]^{\frac{1}{2}} \frac{1}{\left(\frac{N_a}{N_a} + 1\right)}$$

$$x_{p_0} = \left[\frac{2\epsilon V_0}{q}\frac{N_d}{N_a(N_a + N_d)}\right]^{1/2}$$

$$x_{n_0} = \left[\frac{2\epsilon V_0}{q}\frac{N_a}{N_d(N_a + N_d)}\right]^{1/2}$$

if $N_a << N_d$, $x_{p_0} >> x_{n_0}$.

- A deep penetration is necessary in lightly doped material to "uncover" the same amount of space charge as for a short penetration into heavily doped material.

- Transistion width W varies as square root of the potential across the region

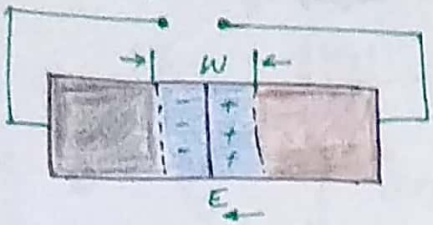
$$W \propto V^{1/2}.$$

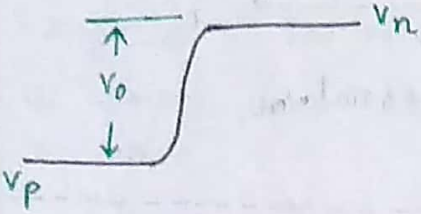
- In derivation we only considered contact potential.

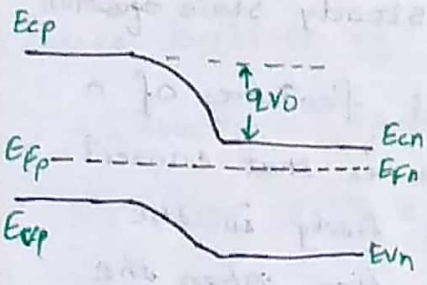
- An applied bias can increase or decrease the potential across the transistion region by

Qualitative description of current flow at a junction.

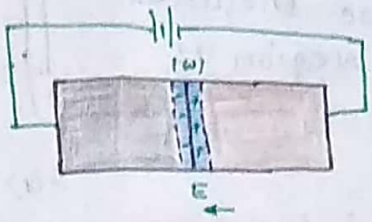
(a) Equilibrium $V=0$

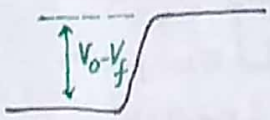


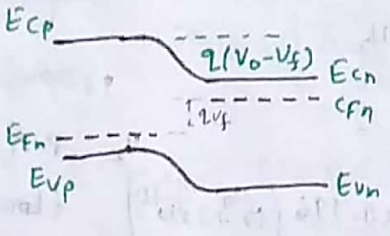




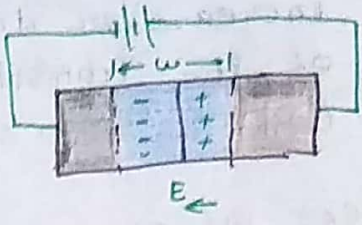
(b) Forward Bias $V=V_f$

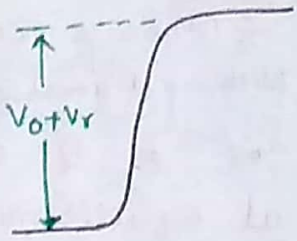


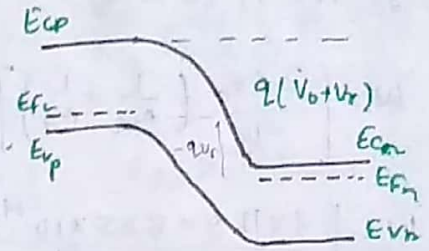


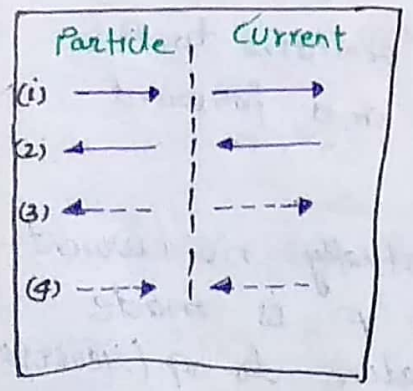


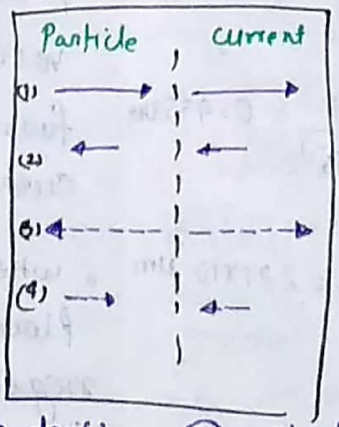
(c) Reverse Bias $V=-V_R$

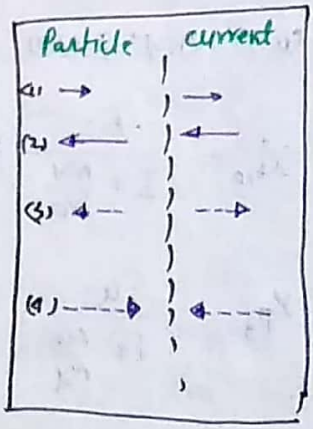












(1) Hole diffusion (2) Hole drift (3) electron diffusion (4) electron drift

- The shape of the band diagram in the depletion region is not linear, but consist of two parabolic curves that join smoothly.

- We assume that an applied voltage bias V appears across the transition region of the junction rather than in the neutral n and p regions.
- There will be voltage drop in the neutral region (material), if a current flows it. but resistance is very small in each area (neutral) and only a small voltage drop outside the space charge region.
- For almost all calculation it is valid to assume that an applied voltage appears entirely across the transition region.
- An applied voltage changes the electrostatic potential barrier and thus the electric field within the transition.
- The seperation of energy band is affected by the applied bias along with width of depletion region.
- The electrostatic potential barrier at the junction is lowered by a forward bias V_f from the equilibrium contact potential V_0 to $(V_0 - V_f)$.
- This lowering of potential barrier occurs because of forward bias V_f raises the electrostatic potential on the p side. relative to the n side.
- for reverse bias $(V = -V_r)$, the electrostatic potential of the p side is depressed relative to n side. and potential barrier becomes $(V_0 + V_R)$.
- The electric field decreases with forward bias. Since applied electric field opposes the built in field.
- with reverse bias the field at the junction is increased by an applied field, which is same direction as the built in field.
- W decreases under forward bias and increases under reverse bias.

$$W = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)(V_0 + V_r)} \quad - R.B.$$

$$W = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)(V_0 - V_f)} \quad - F.B.$$

$$W = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)V_0} \quad - No.B.$$

Unit-3.

Crystal growth : Bulk and epitaxial

Bulk Crystal growth

- The progress of Solid state device technology since the invention of the transistor in 1948 has dependent on
  (i) development of device concept
  (ii) Improvement of materials.
- The requirements on the growing of device grade Sc crystals are more stringent than those for any other materials.
- SC purity must be extremely close limits for example:- Si crystal used in devices are grown with concentrations of most impurities of less than one part in ten billions.
- Such purity require careful handling and treatment of the material at each step of the manufacturing process :

Starting Materials

- The raw feed stock for Si crystal is Silicon dioxide (SiO_2).
- we react SiO_2 with C in the form of coke in arc furnace at very high temperature (1800°C) to reduce SiO_2 according to the following reaction:

$$SiO_2 + 2C \rightarrow Si + 2CO$$

- This forms metallurgical grade Si(MGS).
- MGS which has impurities such as fe, Al and heavy metals at level several hundred to several thousands part per million (ppm).
- while MGS is clean enough for metallurgical applications such as using Si to make stainless steel.
- MGS is not pure enough for electronic applications
- MGS is not single crystal.
- MGS is refined further to yield SC grade or electronic grade Si (EGS)
- EGS level of impurities are reduced to parts per billion. ($1\ ppb = 5 \times 10^{12}\ cm^{-3}$)
- EGS involves reacting the MGS with dry HCl, according to following reaction

$$Si + 3HCl \rightarrow SiHCl_3 + H_2$$

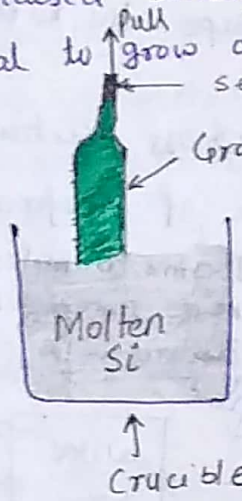
($SiHCl_3$: trichlorosilane)

- $SiHCl_3$ which is liquid with boiling point of 32°C.
- Along with $SiHCl_3$, chlorides of impurities such as $FeCl_3$ are formed which fortunately have boiling points that are different from $SiHCl_3$.
- By fractional distillation, in which we heat up by mixture of $SiHCl_3$ and the impurity chlorides and condense the vapours in different distillation towers held at appropriate temperatures.
- Now seperate pure $SiHCl_3$ from impurities, $SiHCl_3$ is then converted to highly pure EGS by reaction with H_2.

$$2\,SiHCl_3 + 2H_2 \longrightarrow 2\,Si + 6\,HCl$$

Growth of Single-crystal Ingots

- We have to convert the high purity but still polycrystalline EGS to single crystal Si ingots or boules. (99)
- This is done by Czochoralski Method.
- In order to grow single crystal material, it is necessary to have a seed crystal which can provide a template for growth.
- Melt the EGS in a quartz-lined graphite crucible by resistivity heating (99) it to the melting point of Si (1412°C) (11)
- A seed crystal is lowered into molten material and then is raised slowly, allowing the crystal to grow onto the seed.

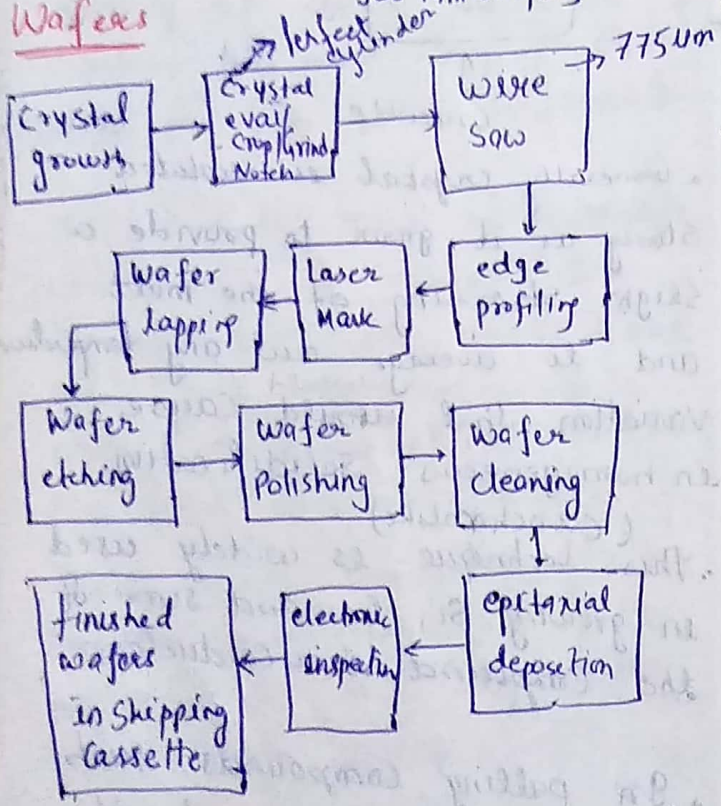


- Generally crystal is rotated slowly as it grows to provide a slight stirring of the melt and to average out any temperature variation that would cause inhomogeneous solidification. (Czochoralski)
- This technique is widely used in growing Si, Ge and some of the compound semiconductors.
- In pulling compounds such as GaAs from the melt, it is necessary to prevent volatile element (e.g. As) from vapourising.
- A layer of B_2O_3, which is dense and viscous when molten, floats on the surface of the molten GaAs to prevent as evaporation.

This growth method is called liquid-encapsulated Czochralski (LEC) growth.

- In Czochralski method, the shape of ignot is determined by a combination of
  (i) polygonal shape due to crystal structure
  (ii) circular cross section due to influence of surface tension. [300 mm diameter Si ingot, 1 m long, 140 kg 300 mm wafer]

Wafers



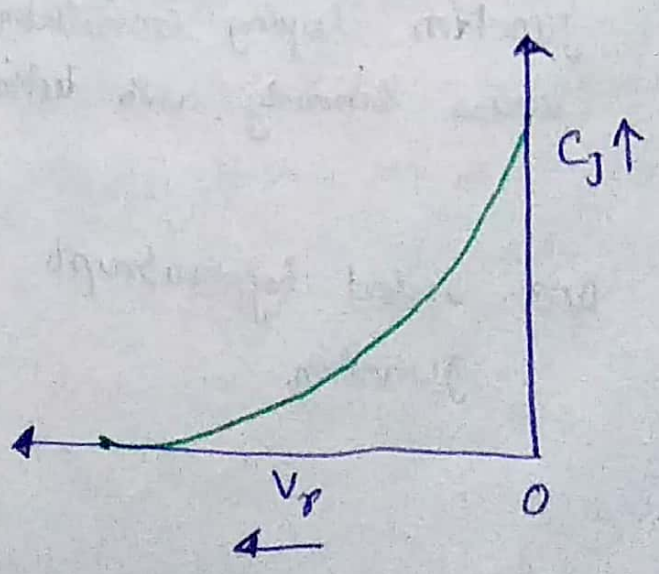
- After the single-crystal ignot is grown, it is then mechanically processed to manufacture wafers.
- The first step involves mechanically grinding the more or less cylindrical ingot into a perfect cylinder with a precisely controlled diameter.
- Next, the Si cylinder is sawed into individual wafers about 775 um thick, by using a diamond tipped inner hole blade saw or a wire saw.
- The resulting wafers are mechanically lapped and ground on both sides to achieve a flat surface and to remove the mechanical damage due to sawing.
- Such damage would have detrimental effects on devices.
- The flatness of the wafer is critical from the point of view of "depth of focus" or how sharp an image can be focussed on the wafer surface during photolithography.
- The Si wafers are then rounded or "chamfered" along the edges to minimize the likelihood of chipping the wafer during processing.
- Finally the wafer undergo chemical-mechanical polishing using a slurry of very fine SiO_2 particles in a basic NaOH solution to give front surface of the wafer

Varactor Diode.

- Varactor is a reverse biased p-n junction diode whose junction capacitance can be varied with the applied reverse bias voltage in a controlled manner.

- The term varactor is derived from the words variable reactor. It is also known as varicap means variable capacitance.

- deplition layer width increases with increase of reverse bias voltage, the increase in depletion layer reduce the junction capacitance of p-n junction diode.



- When the reverse bias voltage decreases, depletion width decreases which in turn increases the capacitance, when the reverse bias is equal to zero, the capacitance becomes maximum.

- The capacitance can be controlled by doping profile such as Abrupt, linearly graded and hyperabrupt doping profiles.

- The general doping distribution can be expressed for one sided heavily doped junction as follows

$$N_d(x) = Ax^m \quad \text{for } x \geq 0$$

A and m are constant for a particular doping profile.

$m = 0 \rightarrow$ one sided abrupt junction with uniform doping.

$m = 1 \rightarrow$ one sided linearly graded junction, doping concentration varies linearly with distance

$m < 0 \rightarrow$ one sided hyperabrupt junction

$$C_J \propto (V_{bi} + V_R)^{-\frac{1}{m+2}}$$

- for abrupt junction

$m = 0 \quad C_J \propto \frac{1}{\sqrt{V_R + V_{bi}}}$

$m = 1$ (linearly graded junction)

$$C_J \propto (V_{bi} + V_R)^{-\frac{1}{3}}$$

- for hyperabrupt junction

$m = -1, -\frac{3}{2}, -5/3$

$C_J \propto \frac{1}{(V_R + V_{bi})}; \frac{1}{(V_R + V_{bi})^2}; \frac{1}{(V_R + V_{bi})^5}$ respectively.

- The voltage sensitivity of capacitance of a varactor diode is defined by

$$S = -\frac{dC_j}{C_j} \cdot \frac{V}{dV} = \frac{1}{m+2}$$

- The larger the value of S, the larger will be the variation of capacitance with reverse bias voltage. Thus the voltage sensitivity is highest for hyperabrupt junction.

$$C_T = \frac{C(0)}{\left(1 + \left(\frac{V_R}{V_T}\right)\right)^n}$$

$n = \frac{1}{2}$ for alloy junction

$\frac{1}{3}$ for diffused junctions.

Unit-9

SCR (Silicon Controlled Rectifier)

Theory of operation, Switching consideration), Unijunction transistor. (Theory of operation)

Unit-9 Specail diodes

Zener diode, Tunnel diode, Varactor diode, Schottky diode, Photo diode (PIN & Avalanche), Solar cells, LED, Solid state Laser diodes.

Unit-10 CCD and CCD Cameras

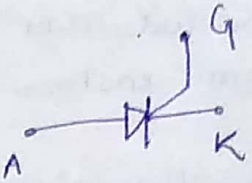
Unit-8

Thyristor:- SCR

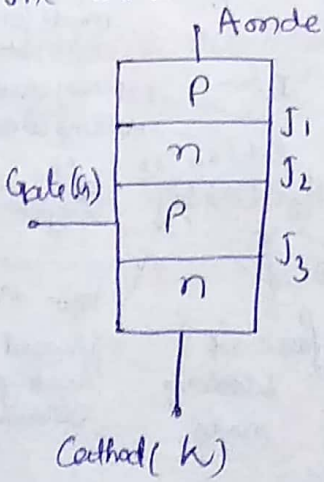
- The name thyristor is derived by a combination of the capital letters from THYRatron and transistor.
- International Electrotechnical commission (IEC) in 1963 decided the definition of Thyristor as under:
  - (i) It constitues three or more p-n junctions.
  - (ii) It has two stable states, an ON-state and off-state and can change its state from one to another.
  - (iii) Thyristor is four layer, three junction, p-n-p-n Semiconductor switching device.

Silicon Controlled Rectifier (SCR)

- SCR is the oldest and first member of the thyristor family. It is called SCR because, Silicon is used for its construction and its operation as a rectifier (very low resistance in forward conduction and very high resistance in the reverse bias direction) and it can be controlled.
- It has three terminals
  - (1) Anode (A)
  - (2) Cathode (k)
  - (3) Gate (G)



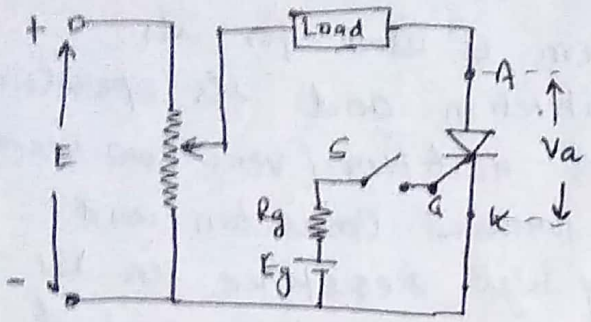
- The structure of SCR



- The terminal connected to outer 'p' region is called Anode (A)
- The terminal connected to outer 'n' region is called Cathode (k).
- The terminal connected to inner 'p' region is called Gate (G).

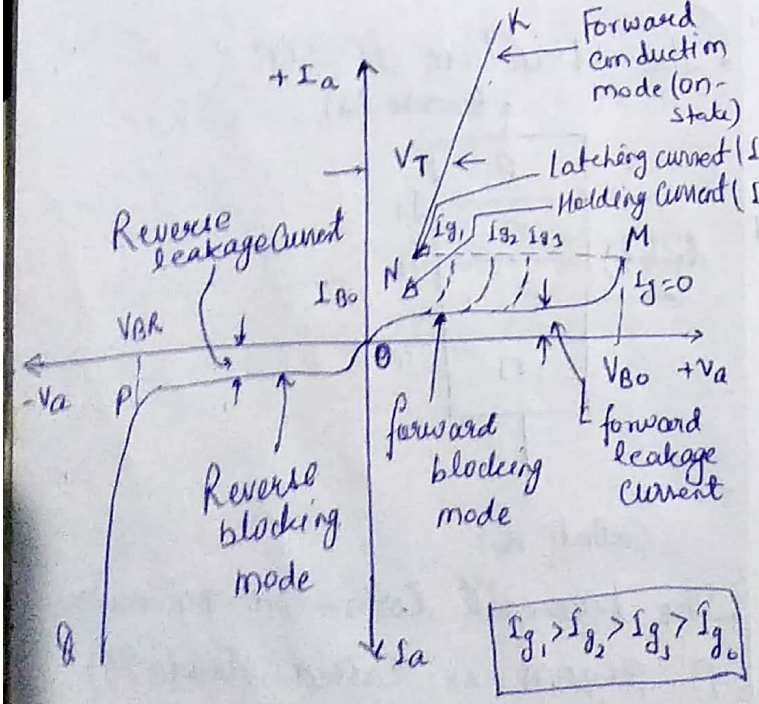
SCR is unidirectional device, it blocks the current flow from cathode to anode.

Static V-I characteristics



- The anode and cathode are connected to main source through the load.
- The Gate and cathode are fed from another source 'Eg'.

V-I characteristic of SCR.



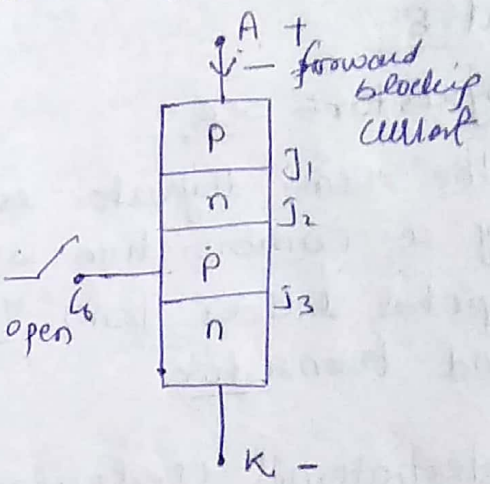
Va = Anode voltage, Ia: Anode current
VBO = forward break over voltage
VBR = Reverse breakdown voltage
Ig = Gate current, IL = Latching current, IH = Holding current

The three basic modes of operation SCR are,

1. Forward Blocking mode
2. Forward Conduction mode
3. Reverse blocking mode

forward blocking mode

- when anode is at a higher potential than cathode, thyristor is said to be forward biased.
- It is seen from the figure that when gate circuit is open J_1, J_3 are forward bias but junction J_2 is reverse bias.



In this mode, a small current, called forward leakage current flows from anode to cathode.

- OM in V-I characteristics represent the forward blocking mode of SCR.
- SCR is treated as an open switch in the forward blocking mode.

Forward Conduction mode

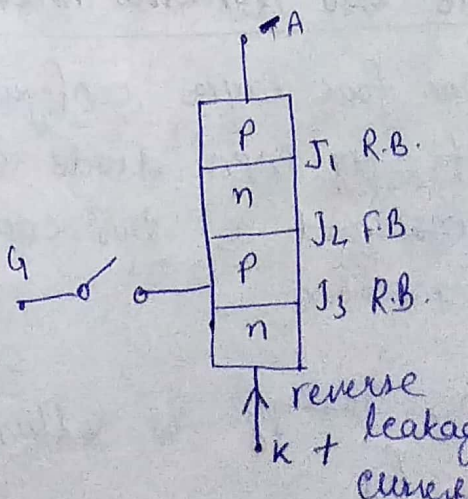
- When anode to cathode forward voltage is increased with gate circuit open, reverse biased junction J_2 will have an avalanche breakdown at a ~~junction~~ voltage called forward break-over voltage V_{BO}.
- After this breakdown, thyristor gets turned ON with point 'M' at once shifting to 'N'. Here NK represents the forward conduction mode.
- A thyristor can be brought from forward blocking mode to forward conducting mode by applying
  (i) A positive gate pulse between gate and anode
  or
  (ii) A forward break over voltage (V_{BO}) across anode and cathode.
- Voltage drop across the SCR 'V_T' increases slightly with increase in anode current. It can be seen from NK.

- **Latching current** :- It is defined as the minimum value of anode current (I_a) which it must attain during turn-on process to maintain conduction when gate signal is removed.
  The gate pulse width should be choosen to ensure the anode current rises above the latching currents.
- **Holding Current** :- It is the minimum value of anode current (I_a) below which the SCR gets turned off.

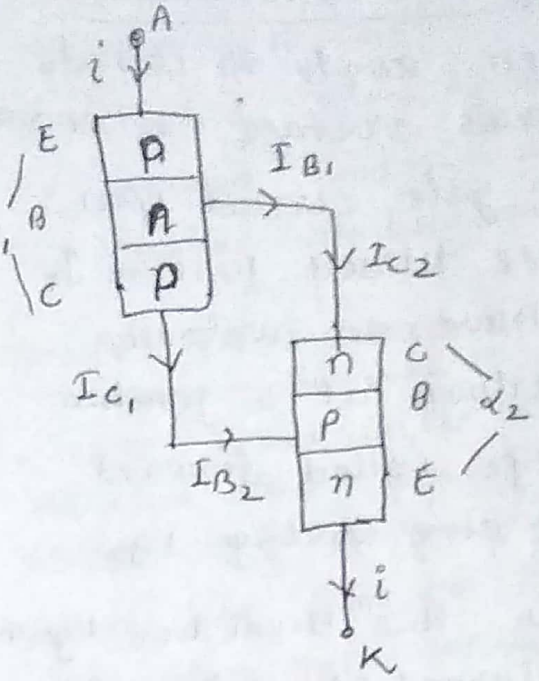
$$I_L > I_H$$

- Latching current is associated with turn on process.
- Holding current is associated with turn off process.

Reverse blocking mode.



- When Cathode is made high Potential with respect to anode with gate open, the the SCR is said to be reverse biased.
- J_1 and J_2 are reverse biased and J_2 as forward bias.
- A small current flow through SCR, this is called as reverse leakage current
- This is reverse blocking mode, called the off state of the scr.
- If the reverse voltage increased, then at reverse breakdown voltage (V_{BR}), an avalanche breakdown occurs at J_1 and J_3 and reverse current increases rapidly (PQ).
- The SCR in the reverse blocking mode may treated as open switch.



- The current I_{C_1} of p-n-p transistor drives the base of n-p-n, the base current of p-n-p (I_{C_2}) drives the collector current of I_{C_2} of n-p-n transistor.
- α_1 for p-n-p transistor, α_2 for n-p-n transistor.

$$I_{C_1} = \alpha_1 I + I_{C_{01}} = I_{B_2} \quad -(1)$$

$$I_{C_2} = \alpha_2 I + I_{C_{02}} = I_{B_1} \quad -(11)$$

$$I = I_{B_2} + I_{C_2}$$

$$I = I_{B_1} + I_{C_2}$$

$$I = (\alpha_1 + \alpha_2) I + (I_{C_{01}} + I_{C_{02}})$$

$$\boxed{I = \frac{I_{C_{01}} + I_{C_{02}}}{1 - (\alpha_1 + \alpha_2)}}$$

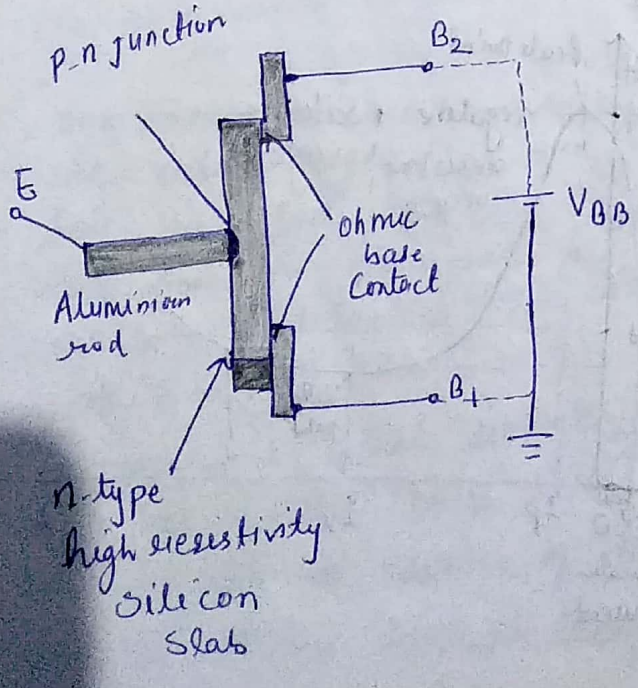
~~Uni junction transistor (UJT).~~

The two transistor Analogy

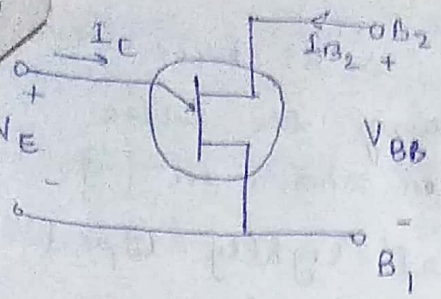
- The four layer configuration of fig pnpn diode can be considered as two coupled transistors.
- The analogy is illustrated in fig

Unijunction Transistor

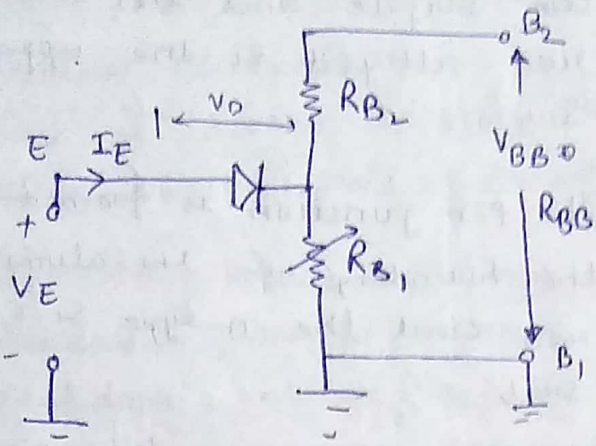
- It is first introduced in 1948, this device did not become commercially available until 1952.
- The low cost per unit combined with the excellent characteristics of the device have warranted its use in a wide variety of applications including
  (i) oscillators
  (ii) trigger circuit
  (iii) Sawtooth generator
  (iv) Phase control
  (v) timing circuits
  (vi) bistable networks
  (vii) Voltage ~~and~~ or current regulated supplies.
- It is a low power absorbing device under normal operating consideration.



- The UJT is a three terminal device having the basic concentration shown in fig.
- A slab of lightly doped (increased resistance characteristics) n-type silicon material has two base contact attached to both ends of one surface and an aluminium rod alloyed to the opposite surface.
- The p-n junction is formed at the boundary of the aluminium rod and the n-type silicon slab.
- The single p-n junction accounts for the terminology unijunction.
- It was originally called duo base diode due to presence of two base contacts.
- The aluminium rod is alloyed to the silicon slab at a point closer to the base 2 contact than the base 1 contact.
- The base 2 terminal is made positive with respect to base 1 terminal by V_{BB} volts.
- The symbol for the unijunction is shown



equivalent circuit: two resistors (one fixed, one variable) and a single diode.



- The resistance R_{B_1} is variable resistance, since its magnitude vary with current I_E.
  R_{B_1} = 5kΩ to 50Ω to corresponding change of I_E from 0 μA to 50 μA.

- The interbase resistance R_{BB} is the resistance of the device terminals B_1 and B_2 when $I_E = 0$.

$$R_{BB} = (R_{B_1} + R_{B_2})\Big|_{I_E = 0}$$

↓ typically (4kΩ to 10kΩ)

- The position of aluminum bead will determine the relative value of R_{B_1} and R_{B_2}.

$$V_{R_{B_1}} = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \cdot V_{BB}$$

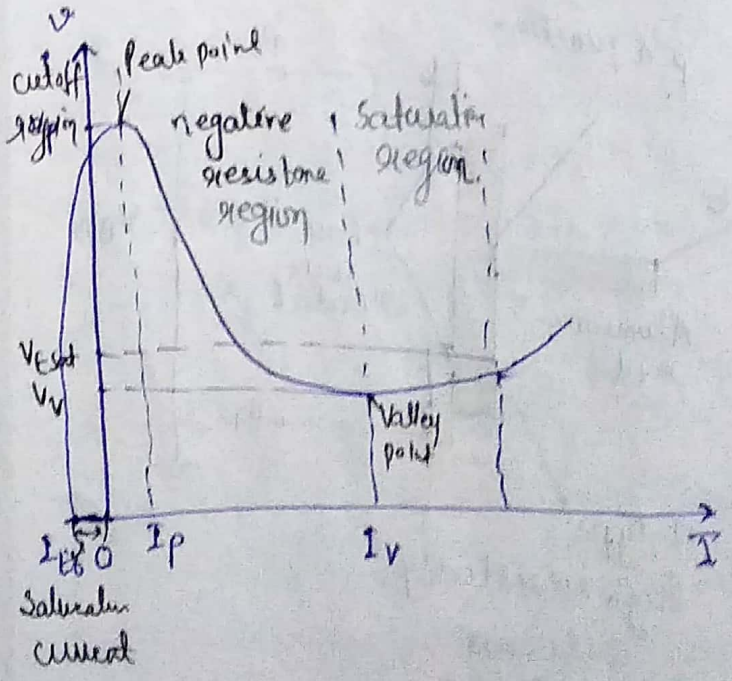
$$\boxed{V_{R_{B_1}} = \eta V_{BB}\Big|_{I_E = 0}}$$

- $\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} = \frac{R_{B_1}}{R_{BB}}$ is called intrinsic stand off ratio

- For applied emitter voltage V_E greater than $V_{R_{B_1}}$ by the forward voltage drop of the diode V_D (0.35 – 0.70V), the diode will fire.

- I_E current will flow, The emitter firing potential is given by

$$V_P = \eta V_{BB} + V_D$$



- for emitter potentials to the left of the peak point, the magnitude I_E is never greater than I_{E0}. The current I_{E0} corresponds very closely the reverse leakage current I_{CO} of bipolar transistor. The region indicated is cut-off region.

- once conduction will start at $V_E = V_p$. the emitter potential will drop with increase in I_E, This corresponds decreasing resistance R_B, for increasing current I_E, has negative resistance region.

- It is stable enough to be used with a great deal of reliability in the area of application listed.

- The valley point will be reached and any further increase in I_E will place the device in the saturation region.

- The decrease in resistance in the active region is due to hole injected into the n-type slab from the aluminium p-type rod when conduction is established.

- The increased hole content in the n-type material will result in an increase in number of free electrons in the slab, producing

In the steady state at thermal equilibrium, the sum of stimulated and spontaneous emission is equal to the absorption rate.

$$(R_{21})_{st} + (R_{21})_{sp} = (R_{12})_{ab}$$

$$\Rightarrow B_{21} n_2 \rho(\nu_{12}) + A_{21} n_2 = B_{12} n_1 \rho(\nu_{12})$$

$$\Rightarrow \rho(\nu_{12}) = \frac{A_{21} n_2}{B_{12} n_2 - B_{12} n_1}$$ A

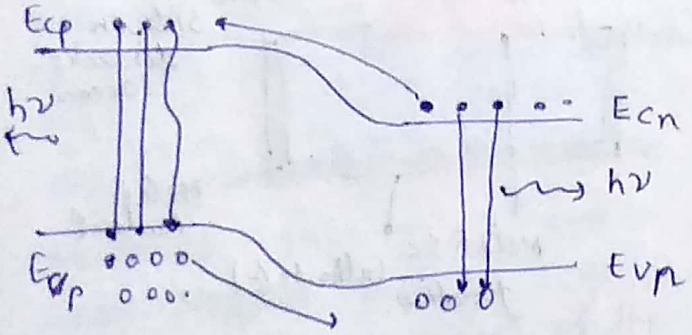
Light Emitting diode.

- LED is an opto electronic or photonic device, which is used as a source of light energy.
- Principle – electroluminescence.
- electroluminescence is the phenomenon of converting electrical energy into light energy which is reverse of photovoltaic effect where light energy is converted into electrical energy.
- It was first discovered by Round in 1904 in SiC point contact rectifier, but light emission was very poor.
- LED is a basically forward bias SC P-n junction device made of suitable materials for emitting light of appropriate wave length.

principle of operation.

- LED wavelength ranges from visible to infrared region of the electromagnetic spectrum depending on the band gap energy of the SC used to fabricate the device.
- The application of forward bias causes injection of minority carriers in the depletion layer.
- The carriers stay in the higher energy state for certain time equal to mean life time, then they recombine and lose energy through spontaneous emission of photons having an energy equal to band gap of SC.
- In forward bias electrons injected from n-type to p type normally occupy empty Conduction band states in p-type material & vice versa.
- Thus a large population of excess minority carriers injected on both sides of the junction diffuse away from the junction and recombine with majority carriers.

- The recombination of electrons in the conduction band with holes in the holes in the valence band is a downward transition process in the energy band diagram so that excess energy is spontaneously emitted in form of light photons or other form of energy.
- The emitted photon in radiative transistion have no definite phase relationship among themselves, so LED is incoherent light source.
- LED is multimode optical source, it is used in optical communication system employing multimode fibres.



LED materials.

- The wavelength of light emission from LED depends on the choice of the base SC material and its band gap energy.

$$h\nu = E_g$$

$$\lambda = \frac{hc}{E_g} = \frac{1.24}{E_g(ev)} (\mu m)$$

- Visible radiation from LED can be obtained if the band gap energy of SC has greater than or equal to 2 ev.
- These wide band gap sc have high resistivity and it is very difficult in practice to dope them heavily.
- elemental SC like Si and Ge have indirect band gaps. so these material are not suitable for fabrication of LED.
- Another wide band gap SC, silicon carbide (SiC) may be used for fabrication LED emitting visible light.
- P-n junction based on SiC, emitting blue light is commercially available.
- using dopants like B, Al Se and Be respectively yelbw, blue, green, and red light emission is possible from SiC LED.
- SiC has high melting point, and wide band gap and indirect band gap sc. Therefor low radiative efficiency.

1. (i) Temperature and energy band gap

(ii) $(Volt)^{-1}$

(iii) 2.25×10^{15} atom/cm^3, 10^5 atom/cm^3

(iv) doping

(v) electric field and carrier concentration

(vi) 1.127 μm

(vii) carrier life time and forward current.

(viii) Metal oxide field effect Transistor

(ix) Insulated gate field effect Transistor.

(x) Second quadrant.