ANSWERS OF 'MICROPROCESSOR & ITS APPLICATIONS" MID-SEM PAPER (NOV-2018)

1 (i) d
(ii) C
(iii) a
(iv) C
(v) d

2. (i) $\overline{LOCK}$ → It is an active Low signal. It indicates to another system bus master, not to gain control of the system bus while LOCK is active.

(ii) MN/$\overline{MX}$ → This pin indicates what mode the processor is to operate in.

In minimum mode, 8086 itself generates all bus control signals.

In maximum mode, the three status signals are to be decoded to generate all the bus control signals.

(iii) HOLD → HOLD indicates that another master is requesting a local bus "HOLD". To be acknowledged, HOLD must be active HIGH. On receiving HOLD signal, µP will issue HLDA (High) as an acknowledgement in the middle of T1 clock cycle.

(iv) $\overline{TEST}$ → This ~~TEST~~ Pin is examined by the "WAIT" instruction. If the TEST pin is Low, execution continues. Otherwise, the µP waits in an "idle" state.

(v) AD_0-AD_{15} → These lines constitute the time multiplexed memory/IO address during the first clock cycle (T1) and data during T2, T3 & T4 clock cycles.

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(3)

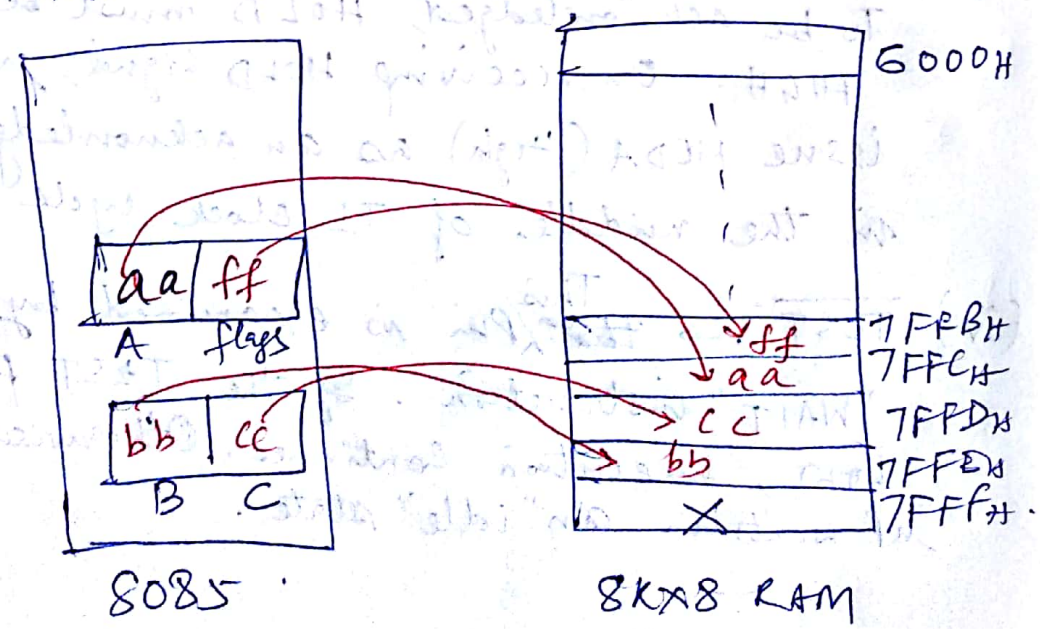
No. of T-states		
10 T	6000_H :	LXI SP, $7FFF_H$.
12 T	6003_H :	PUSH B ; B & C saved on stack.
12 T	6004_H :	PUSH POP ; A & flags saved on stack
10 T	6005_H :	POP B ; B ← A, C ← flags.
4 T	6006_H :	MOV A, C ; A ← flags
10 T	6007_H :	OUT 01_H ; port address : 01_H (assume)
4 T	6009_H	MOV A, B ; A ← A :
10 T	$600A_H$.	POP B ; B ← B ; C ← C
	$600B_H$:	HLT

total: 72 T

Clock freq = 5 MHz.

⇒ $1T = \frac{1}{5}\ \mu s = 0.2\ \mu s$

⇒ total execution time = $72 \times 0.2 = 14.4\ \mu s$



(4)(i) Addressing modes of 8085:

(a) Register addressing → In this mode, the data is copied from one register to another. eg: MOV B,C.

(b) Immediate addrng → In this mode, 8/16 bit data is specified in the instruction itself as one of the operand. eg: MVI C, 0A$_H$.

(c) Direct addressing → In this mode, the data is directly copied from the given address to the register. eg: LDA 2750$_H$; means data is copied from [2750$_H$] to Accumulator.

(d) Indirect addressing → In this mode, the data is transferred from one register to another by using the address pointed by the register. eg: LDAX B ; means data is copied from the address location pointed by BC register pair to Accumulator.

(e) Implicit addressing → This mode doesn't require any operand. The data is specified by the opcode itself. eg: CMP, etc.

PTO

4(ii) Program to get smallest number in data array.

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        LXI H, 3000H   ; set pointer for array
        MOV B, M       ; load the count
        INX H
        MOV A, M       ; set 1st element as smallest data
        DCR B          ; Decrement count
Loop:   INX H          ; increment HL to point to
                       the next element in array.
        CMP M          ;
        JC Ahead       ; if A < M goto ahead
        MOV A, M
Ahead:  DCR B
        JNZ Loop
        STA 4000H      ; Store the smallest data
                       at 4000H.
        HLT.
```

5(i) Pending interrupt → A pending interrupt is simply an interrupt that has occured, is enabled but hasn't made it through the interrupt prioritization process to have its handler executed. 8085 µP has 5 interrupts and only one interrupt may occur during Interrupt service subroutine and other interrupts remain pending.

SIM instruction: It is a multipurpose instruction used for the following purposes:

(a) Serial data transfer (Serial o/p data)
(b) Masking interrupts.
(c) Reset interrupt pending flag

(ii) RIM instruction: It is also a multipurpose instruction used for the following purposes.

(a) Serial data transfer (Serial i/p data)

(b) Read the pending interrupts.

(c) Read the interrupt enable flag (ie whether the interrupts are enabled or not).

(d) Mask status of interrupts.

Note: For 2-5 marks this much description is enough. But for University exams, you also need to write format of SIM and RIM instructions. (This can be found in any book on 8085).

5(ii) DMA Controller → DMA stands for Direct Memory Access. ~~It is design~~ It allows the device to transfer data directly to/from memory without any interference of CPU. Using a DMA Controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from CPU.

Intel 8257 → It is a 40 pin IC used as a programmable DMA controller. i.e. it is a device to transfer the data directly between I/O and memory without through the CPU.

8257 has four channels and hence it can be used to provide DMA to 4 I/O devices. Each channel can be independently programmable to transfer upto 64 KB of data by DMA.

Note: For univ. exam., plz give functional blocks and format of mode set register. Here for 2.5 marks, u don't need to give so much details.