MUZAFFARPUR INSTITUTE OF TECHNOLOGY, MUZAFFARPUR, BIHAR – 842003

(Under the department of Science & Technology, Bihar, Patna)

B. Tech. (ECE) IV Semester Mid-Semester Examination, 2018

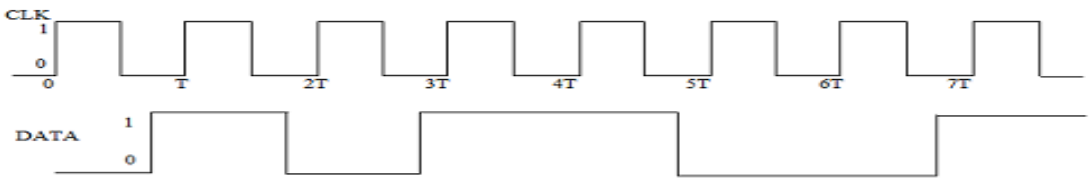
Digital Electronics

Time: 2 hours **Full Marks: 20**

Instructions: Attempt any three questions. Question 1 is compulsory. The number of marks carried by a question/part is indicated against it.

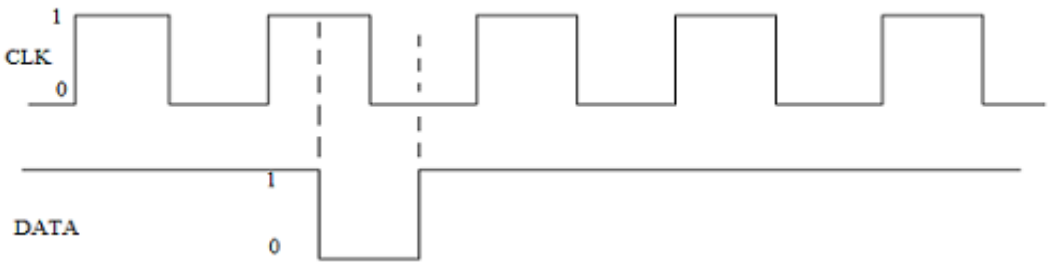
Attempt Question No. 1 for 10 Marks only.

1. (A) Convert the following numbers as required:- (1)
   (i) $(ABCD)_{16}=(\ )_2$
   (ii) $(CAFE)_{16} = ()_8$
   (B) Minimize the Boolean function, Y= A'B'C'+A'BC'+A'BC+ABC' using Boolean theorem. (1)
   (C) What is the significance of the equation $\mathbf{C_{i+1} = G_i + P_iC_i}$ in relation to Carry Look Ahead Adder? Define Gi and Pi. (1)
   (D) Implement the logic function Y= AB+CD using diodes and resistors. (1)
   (E) Implement OR logic function using transistor. (1)
   (F) Simplify using K-Map: F(A,B,C,D) = Σ m(0,1,2,4,8,9,12,14) +Σ d(5,6,13). Implement the simplified expression with AND-OR logic. (2)
   (G) For the given function F(A,B,C)= Σ m(0,1,3,6,7), Find Implicant, Prime Implicant and Essential Prime Implicant. (2)
   (H) Implement Y= AB+CD using minimum number of 2-input NAND gates. (2)
   (I) In a 3-input NAND gate, two inputs are to be used. What are the best option available for the unused inputs and which one is the best and why? (2)
   (J) Consider a D-Flip Flop that triggers only on positive going transitions. Draw the output at Q for the given D-input and clock waveforms as shown. (2)



2. (A) Implement the given logic using 8x1 multiplexer
   F(A,B,C) = Σm (0,1,2,3,4,10,11,14,15) (2)
   (B) Convert JK-Flip Flop to T-Flip-Flop by using characteristic and excitation table. (2)
   (C) Write down the expression (A>B, A=B & A<B) only of 4-bit magnitude comparator. (1)

3. (A) What is Priority Encoder? Write truth table, simplify the logic expression using K-map and implement the circuit using basic gates of priority encoder. (2.5)
   (B) Draw the diagram of a 4-bit shift register using J-K Flip-Flop. Each Flip Flop triggers on the negative going transition. Draw the output waveform for all flip-flops when the input data and clock signals are as shown. (2.5)



4 (A) Implement Full Subtractor using a 3 to 8 Decoder. (2)

(B) Draw the state transition diagram of SR-Flip Flop, J-K Flip-Flop, D-Flip-Flop and T-Flip-Flop. (1.5)

(C) Prove NOR gate is a universal gate? Implement E-XOR and E-XNOR using minimum number of NOR Gate only. (1.5)

5. (A) What is race around condition in J-K Flip-Flop. What are the conditions to avoid race around condition. (2)

(B) The truth table for A-B Flip-Flop is shown below. Implement the the sequential circuit using J-K Flip-Flop.

A_n	B_n	Q_{n+1}
0	0	Q'_n
1	0	Q_n
0	1	1
1	1	0

(3)

MID SEMESTER ECE 4th sem - 2019

DIGITAL ELETRONICS

Solutions

1. (A) (I) $(ABCD)_{16} \longleftrightarrow (1010\ 1011\ 1100\ 1101)_2$
A B C D

(II) $(CAFE)_{16} \longleftrightarrow (1100\ 1010\ 1111\ 1110)_2$
C A F E

$(145376)_8$

(B) $Y = \bar{A}'\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C}$

$= \bar{A}\bar{C}(\bar{B}+B) + \bar{A}BC + AB\bar{C}$ $(B+\bar{B}=1)$

$= \bar{A}\bar{C} + \bar{A}BC + AB\bar{C}$

$= \bar{A}(\bar{C}+BC) + AB\bar{C}$

$= \bar{A}(\bar{C}+\bar{C})(\bar{C}+B) + AB\bar{C}$ {Distribution Theorem $(A+BC) \leftrightarrow (A+B)(A+C)$}

$= \bar{A}.(\bar{C}+B) + AB\bar{C}$ $\{(C+\bar{C})=1\}$

$= \bar{A}\bar{C} + \bar{A}B + AB\bar{C}$

$= \bar{C}(\bar{A}+AB) + \bar{A}B$

$= \bar{C}\{\bar{A}+A)\{\bar{A}+B\} + \bar{A}B$ {Distubution Theorem}

$= \bar{C}(\bar{A}+B) + \bar{A}B$

$= \bar{A}\bar{C} + B\bar{C} + \bar{A}B$

(C) $C_{i+1} = A_iB_i + (A_i \oplus B_i)C_i$

$= G_i + P_iC_i$

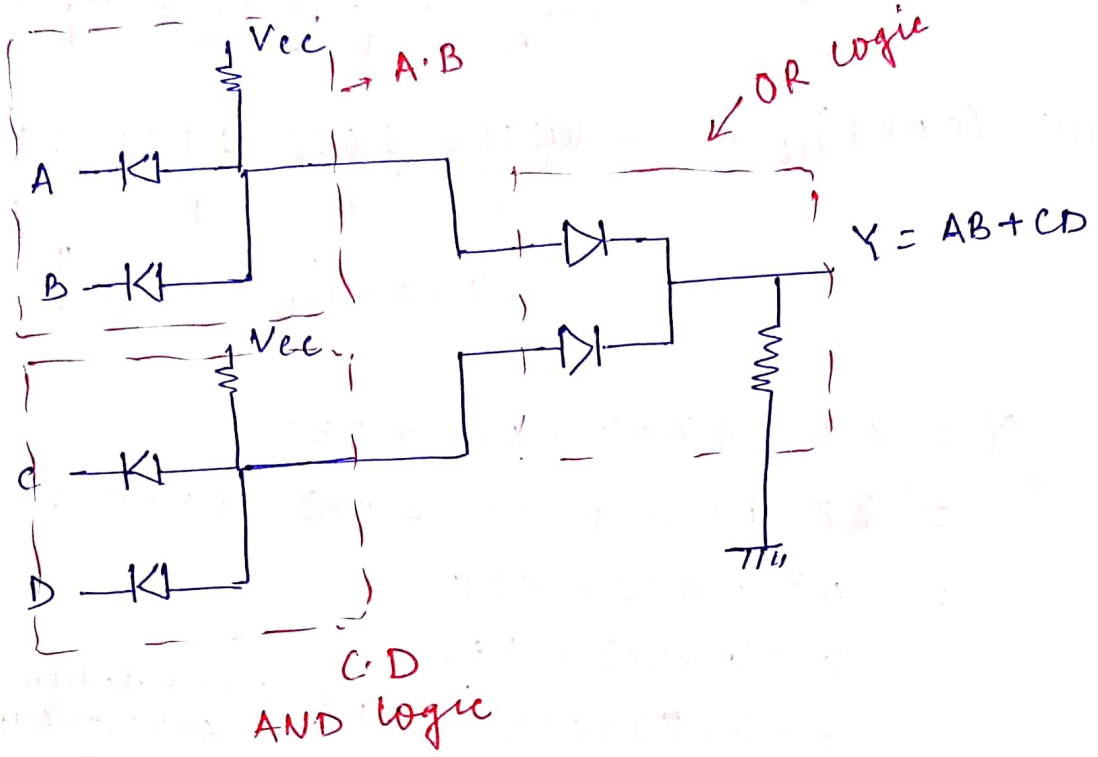
$G_i = A_iB_i \rightarrow$ Generation term.

$P_i = A_i \oplus B_i \rightarrow$ carry propagation term

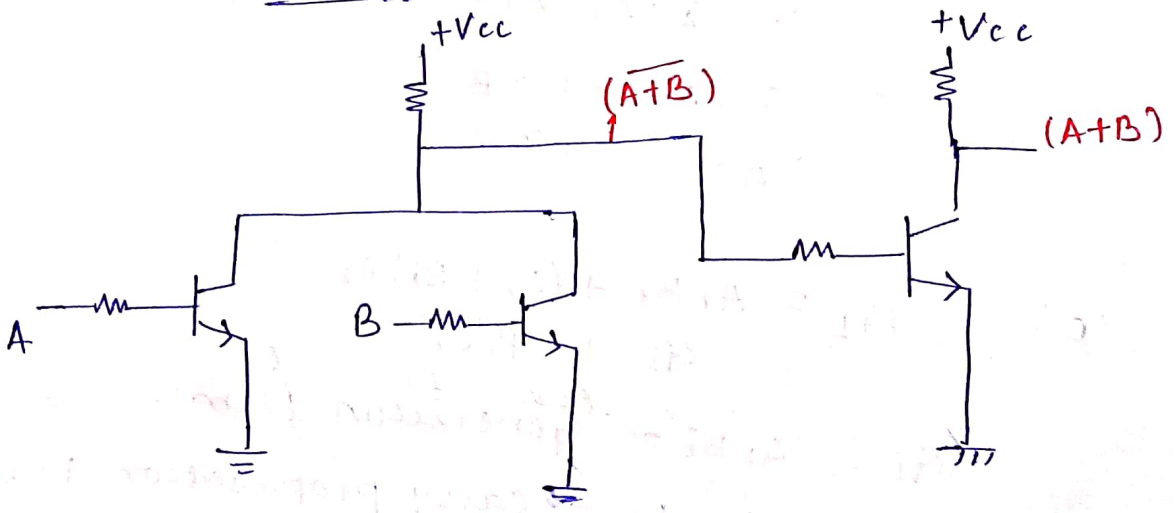
A_i and B_i are the two bits to be added in i^{th} stage of multi-bit adder.

The parameter G_i & P_i are used to predict C_o of each stage if A & B stage is known using c_i of the first stage. The equation $C_{i+1} = G_i + P_i C_i$ is used to predict the carry out of ith stage if the carry-in of that stage is known, which in turn can be predicted recursively from the 1st stage.

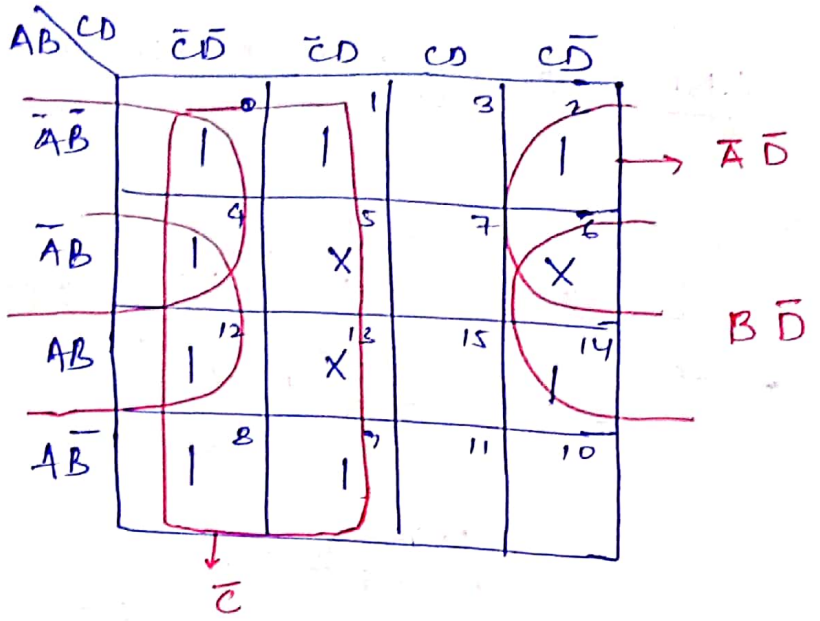
(D) $Y = AB + CD$



(E) OR logic using transistor.

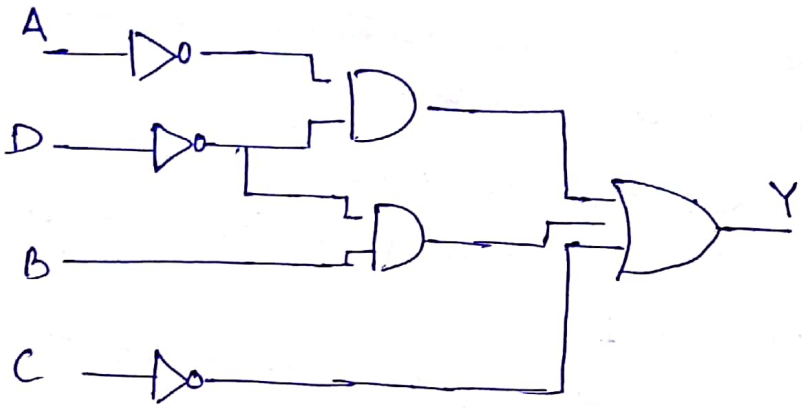


(F) $F(A,B,C,D) = \Sigma m(0,1,2,4,8,9,12,14) + \Sigma d(5,6,13)$

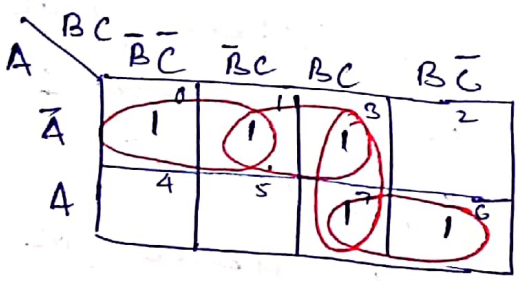


$Y = \bar{A}\bar{D} + B\bar{D} + \bar{C}$

Implementation using Basic gates



(G) $F(A,B,C) = \Sigma m(0,1,3,6,7)$



Implicant:-
$\bar{A}\bar{B}\bar{C}, \bar{A}\bar{B}C, \bar{A}BC, AB\bar{C}$ & ABC

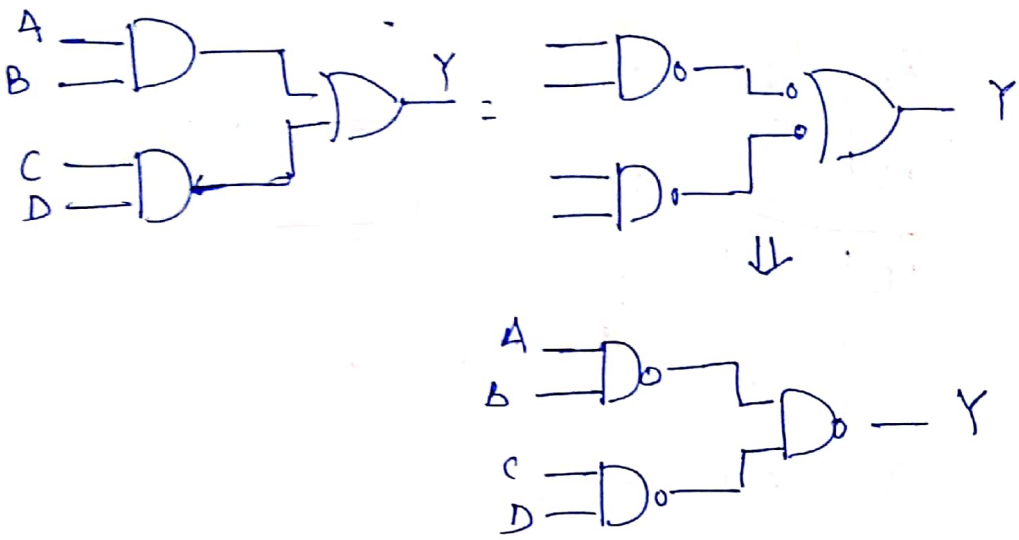
Prime Implicant:-
$\bar{A}\bar{B}, \bar{A}C, AB, B\bar{C}$

Essential prime Implicant
$\bar{A}\bar{B}, AB$

Ie I - 05
PI - 04
EPI - 02

H) $Y = AB + CD$ using minimum no° of NAND gate

AND - OR Logic = NAND - NAND logic



I) 3-Input NAND gate, two inputs are to be used.

There are three options available for the unused inputs.

(I) The ~~unused~~ unused inputs are connected to +5V through resistor so that the logic level is 1.

(II) The unused inputs are tied to a used input.

(III) If NAND gate is fabricated using TTL logic, the unused input can be left as de-connected (open/float). since TTL logic behaves as logic 1 in case of open circuited / floated.

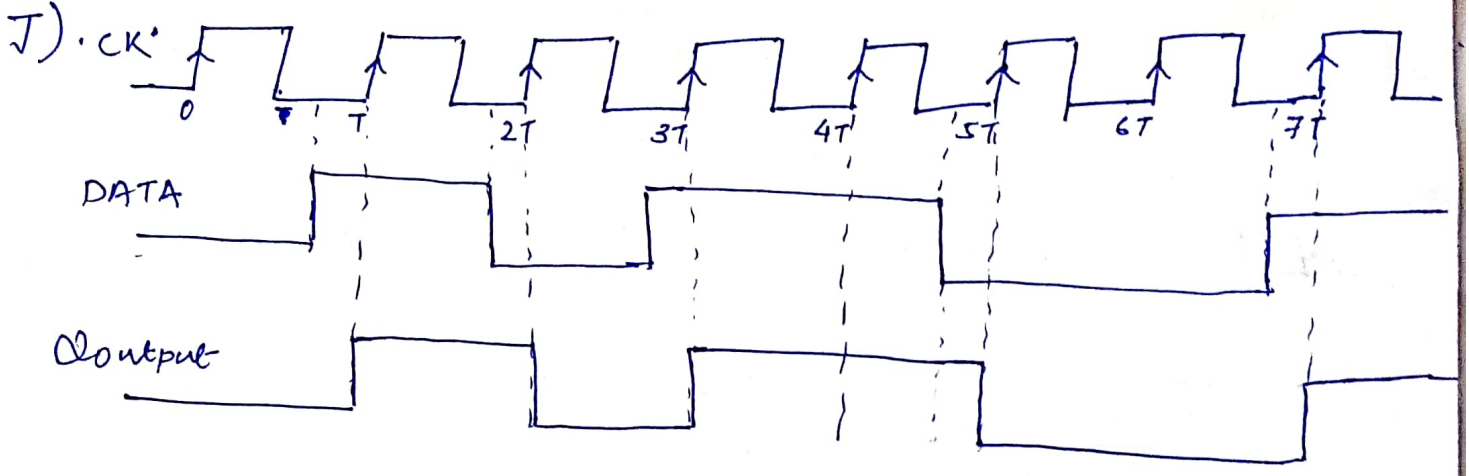
Best option from the above for unused inputs:-

It is not desirable to keep the input floated/open circuited since it act as an antenna

which may pick up stray radiated signal that may cause improper operation of gate.

→ when inputs are tied together, it increases no of driving input and this will lead to decrease effective fanout.

→ So the best option is to connect these inputs to +5V through resistor.

J). 

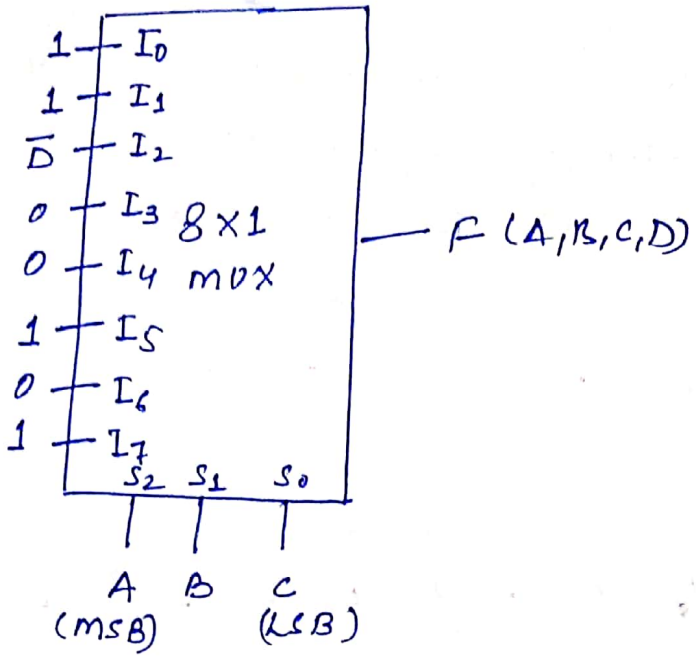
2. (A) $F(A,B,C) = \Sigma m(0,1,2,3,4,10,11,14,15)$

Let A, B, C be the select line

	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}B\bar{C}$	$\bar{A}BC$	$A\bar{B}\bar{C}$	$A\bar{B}C$	$AB\bar{C}$	ABC
D	1	1				1		1
$\bar{D}$	1	1	1			1		1
	1	1	$\bar{D}$	0	0	1	0	1

$$F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD + AB\bar{C}\bar{D} + ABCD$$

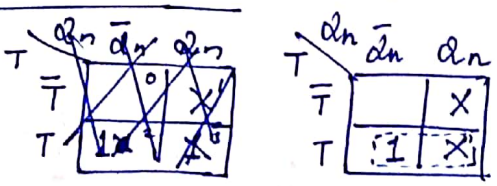
Hence the required 8×1 mux



2.8 (B) JK flip-flop to T-flip-flop.

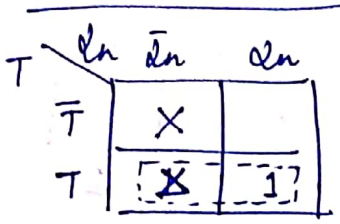
T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

K-map for J



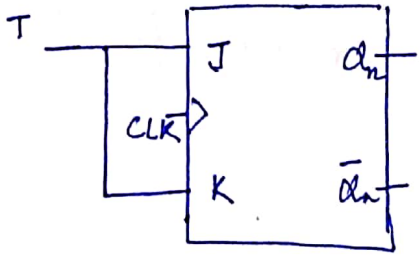
J = T

K-map for K



K = T

Hence Req'd T-FF using JK-FF as below

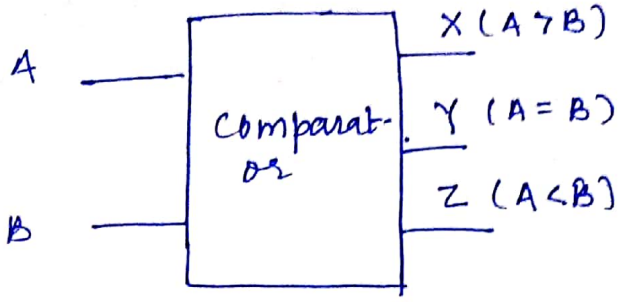


2. (C) The expression for 4-bit magnitude comparator

Let 4-bit no's are

$A = A_3 A_2 A_1 A_0$

$B = B_3 B_2 B_1 B_0$



For X (A > B)

$$A_3\bar{B}_3 + A_2\bar{B}_2(A_3 \odot B_3) + A_1\bar{B}_1(A_3 \odot B_3)(A_2 \odot B_2) + A_0\bar{B}_0(A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)$$

For Y (A = B)

$$(A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)$$

For Z (A < B)

$$\bar{A}_3 B_3 + \bar{A}_2 B_2(A_3 \odot B_3) + \bar{A}_1 B_1(A_3 \odot B_3)(A_2 \odot B_2) + \bar{A}_0 B_0(A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)$$

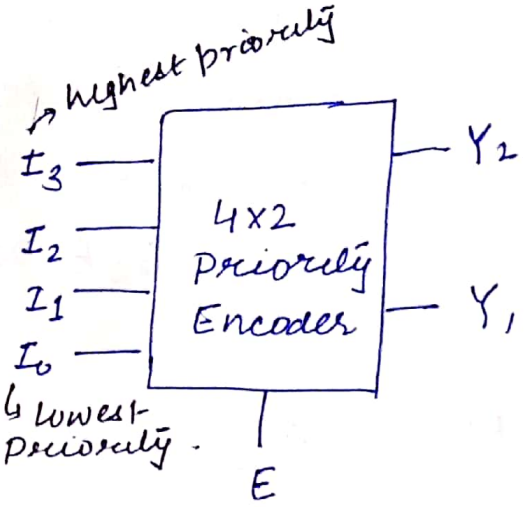
3) (A) Priority encoder:- It is a combinational circuit that generates a specific code at its output corresponding to the currently active inputs which has the highest priority.

→ when an input with a higher priority is present, all other inputs with a lower priority will be ignored / don't care.

Let us consider 4×2 priority encoder having I_3 has highest and I_0 has lowest priority.

$I_1 I_2 I_3 I_4$ are inputs

$Y_2 Y_1$ are outputs

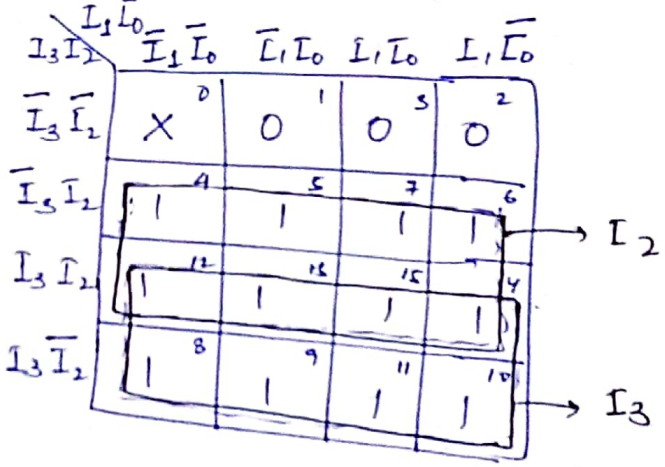


Truth Table

I_3	I_2	I_1	I_0	Y_1	Y_0
0	0	0	0	x	x
0	0	0	1	0	0
0	0	1	x	0	1
0	1	x	x	1	0
1	x	x	x	1	1

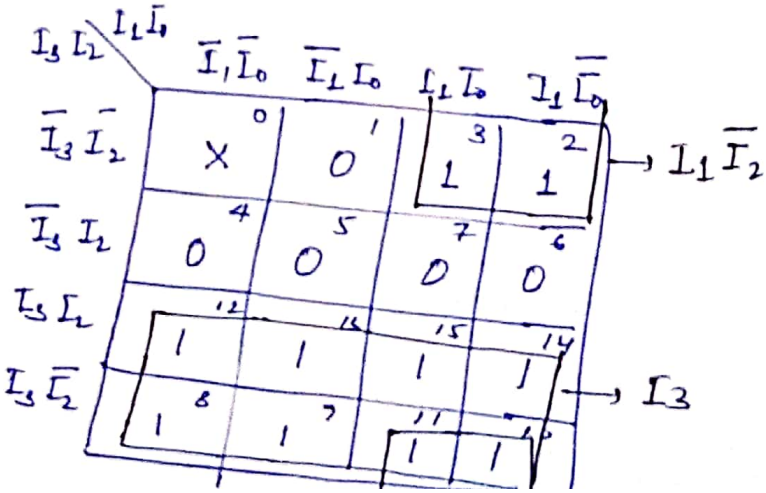
K-map for Y_1

$Y_1 = I_2 + I_3$

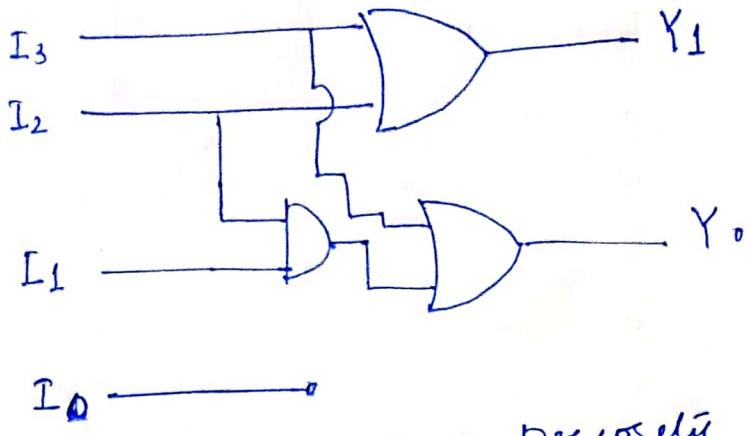


K-map for Y_2

$Y_0 = I_1\bar{I}_2 + I_3$

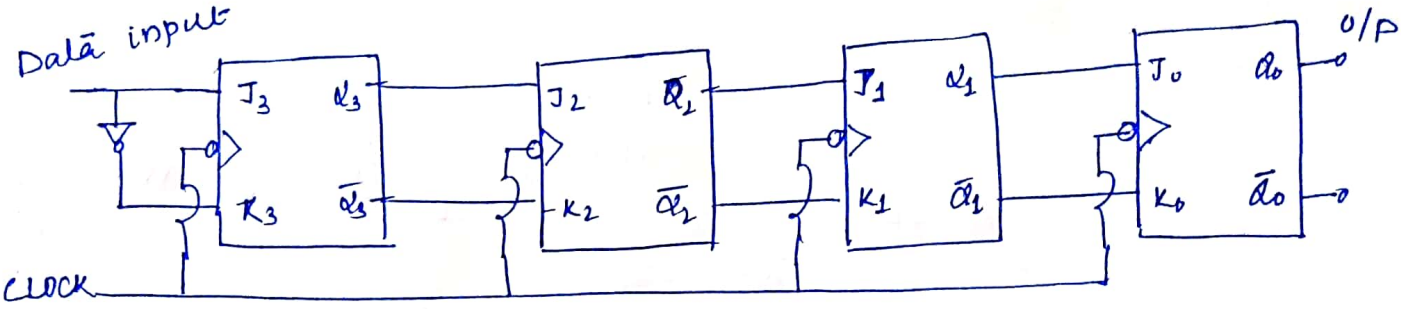


Hence required logic circuit as below

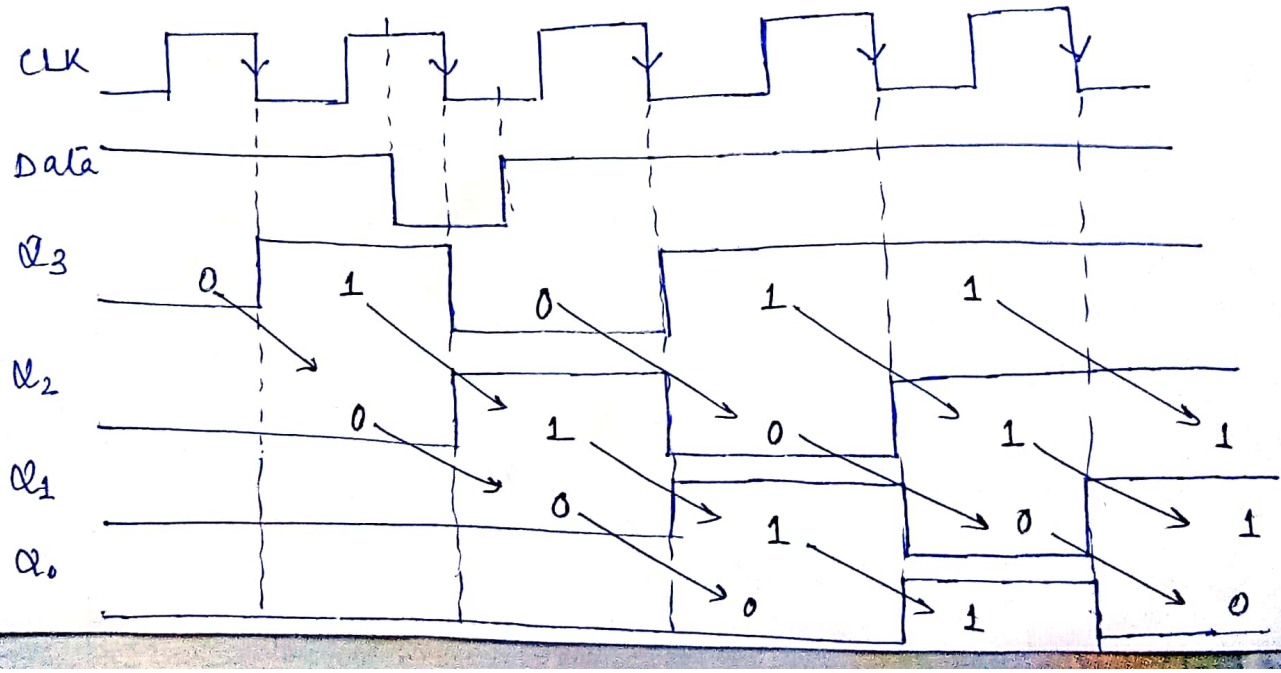


4 x 2 Priority Encoder

3. (B) 4-bit shift register using J-K flip-flop.



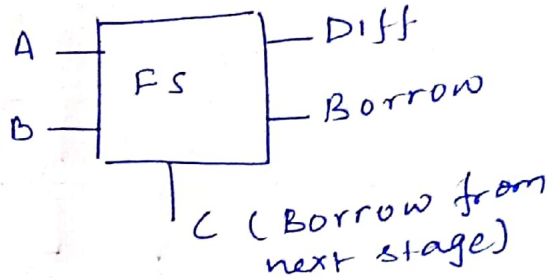
The output waveform of all flip flops for the given data with clock pulse as below:-



4. (A) Full subtractor using 3 x 8 Decoder.

T.T

A	B	C	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



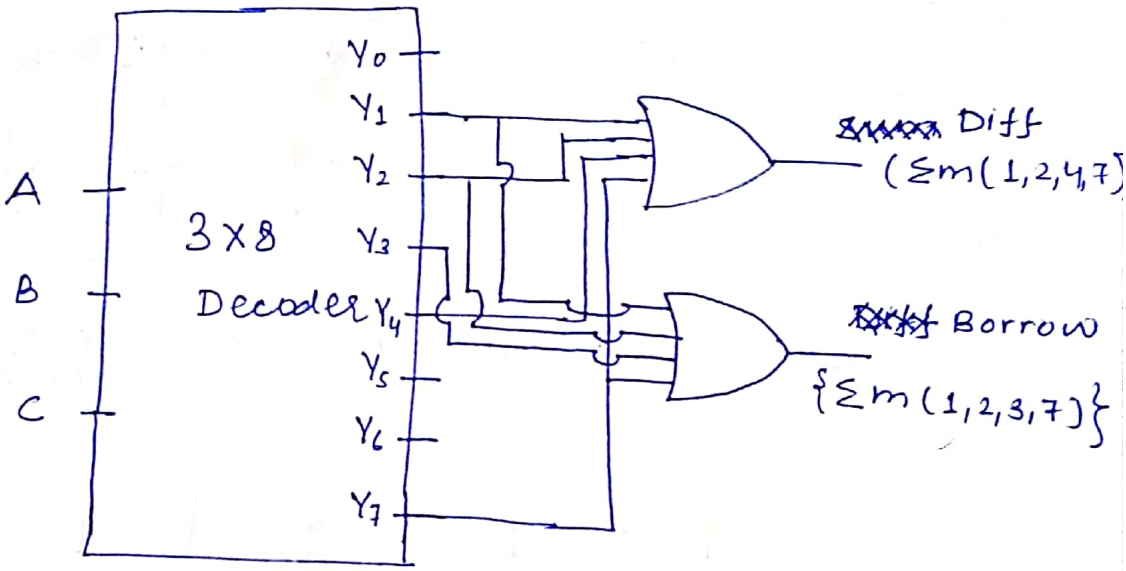
$Diff = \Sigma m(1,2,4,7)$

$= A \oplus B \oplus C$

$Borrow = \Sigma m(1,2,3,7)$

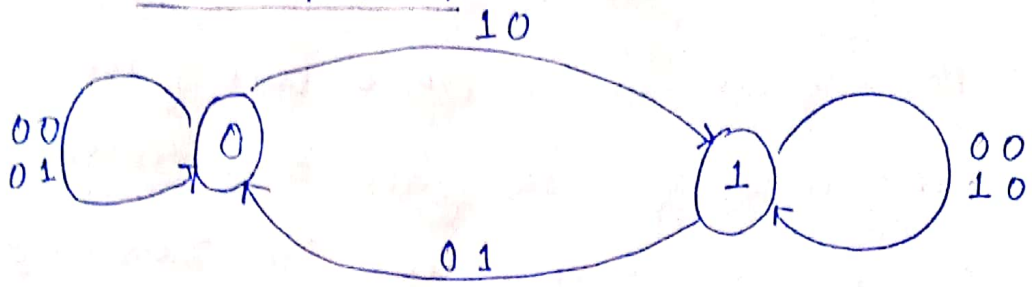
$= \bar{A}B + \bar{A}C + BC$

3 x 8 Decoder

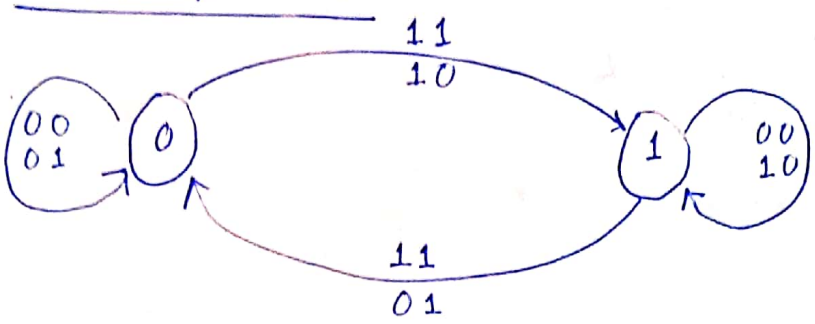


4 (B) Transition Diagram

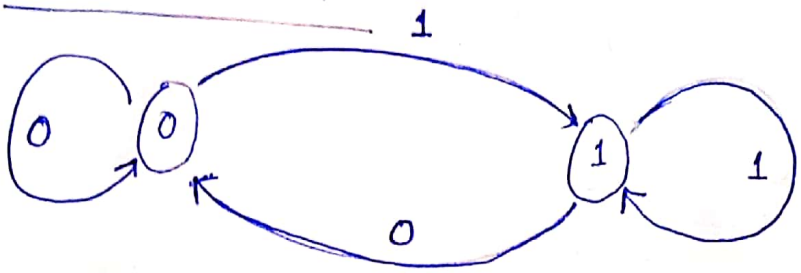
S-R Flip Flop



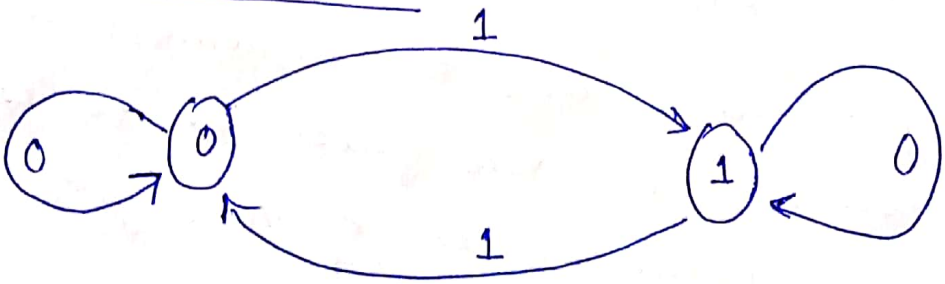
J-K Flip Flop



D - Flip Flop

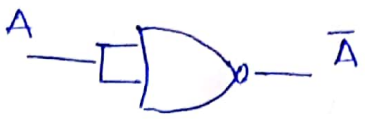


T- Flip Flop

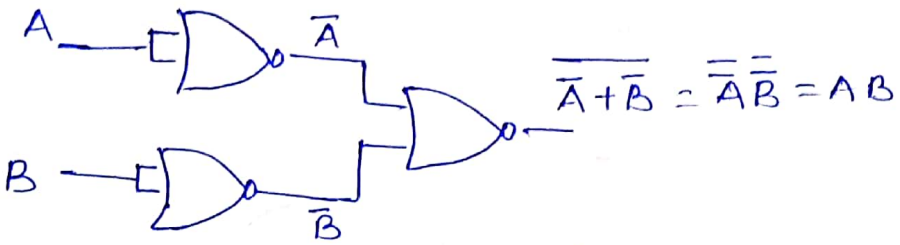


4(C) NOR gate is a universal gate because combination of NOR gate can result into any of the basic gates (AND, OR and NOT)

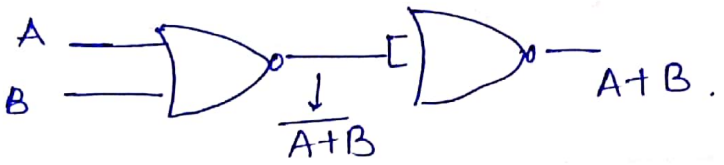
NOT Gate Using NOR



AND Gate Using NOR

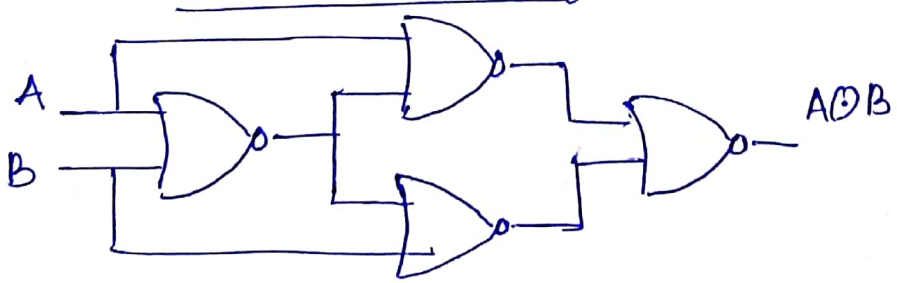


OR Gate Using NOR

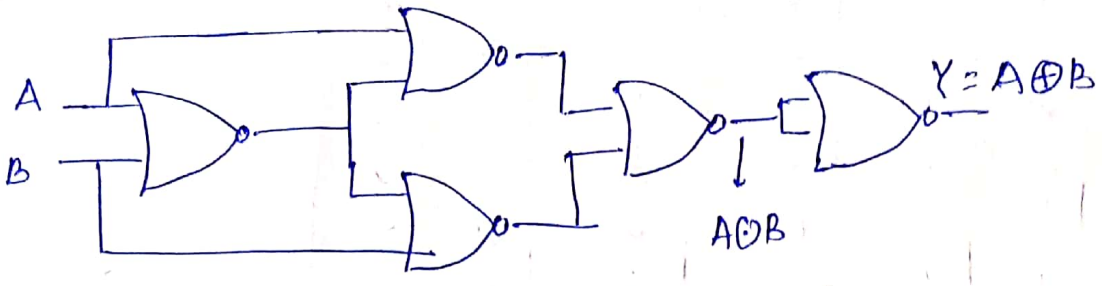


Basic gates are used to implement any logic expressions and basic gates can be implemented by using combination of NOR gate. Hence NOR gate is called universal gate.

EX-NOR Using NOR Gate



EXOR Using NOR gate



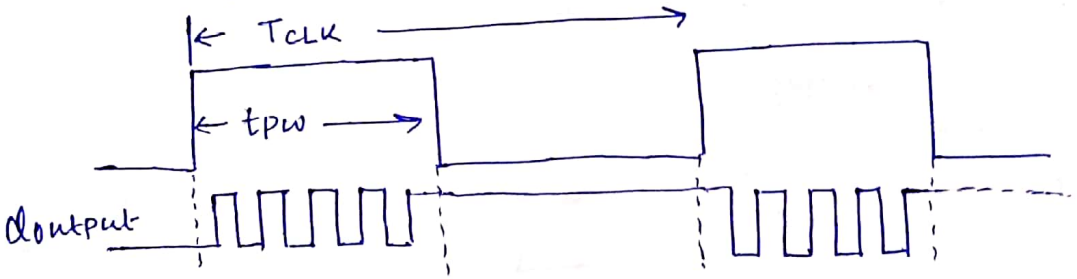
5 (A) Race Around Condition:-

In J-K flip flop, race around condition occurs when J and K inputs are 1 and $t_{pdff} < t_{pw}$ where

t_{pdff} - Propagation delay of flip-flop.

t_{pw} - Pulse width of clock.

During race around condition, output will change many times in 1 clock pulse which leads to uncertainity in determining output state of flip-flop.



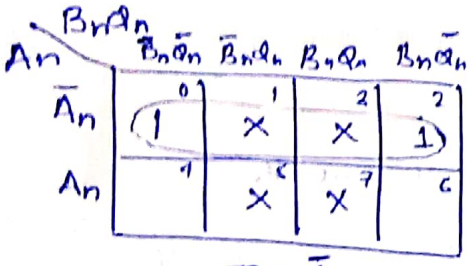
Condition to avoid race around

1. $t_{pw} < t_{pdff} < T_{CLK}$.
2. Edge trigger.
3. Master slave flip-flop.

5 (A)

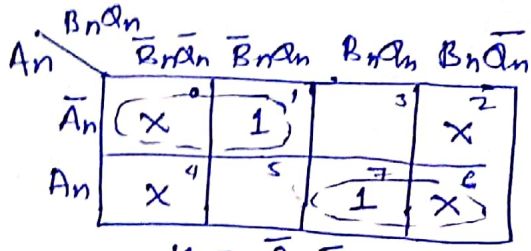
A_n	B_n	Q_n	Q_{n+1}	J	K
0	0	0	1	1	X
0	0	1	0	X	1
0	1	0	1	1	X
0	1	1	1	X	0
1	0	0	0	0	X
1	0	1	1	X	0
1	1	0	0	0	X
1	1	1	0	X	1

K map for J



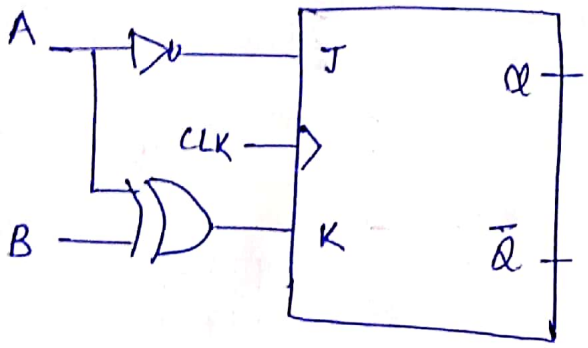
$J = \bar{A}_n$

K-Map for K



$K = \bar{A}_n\bar{B}_n + A_nB_n = A_n \odot B_n$

Hence the required A-B flip flop as follows:-



A-B flip-flop