

SESSION 2024 onwards

SEMESTER- III

Sl No.	Course Code	Course Title	Hours Per Week			Total Credits	ESE	IA
			Lecture	Tutorial	Practical			
1.	106301	Digital Electronics	3	0	0	3	70	30
2.	106302	Data Structure and Algorithm	3	0	0	3	70	30
3.	106303	Object Oriented Programming using C++	3	0	0	3	70	30
4.	106304	Discrete Mathematics and Graph Theory	3	1	0	4	70	30
5.	106305	Operating System	3	0	0	3	70	30
6.	106306	Universal Human Values	3	0	0	3	70	30
7.	106307	Indian Knowledge System	3	0	0	0	-	-
8.	106301P	Digital Electronics Lab	0	0	2	1	30	20
9.	106302P	Data Structure and Algorithm Lab	0	0	2	1	30	20
10.	106303P	Object Oriented Programming using JAVA Lab	0	0	2	1	30	20
11.	106305P	Operating System Lab	0	0	2	1	30	20
12.	106308	Internship-I	2 Weeks			2	30	20
TOTAL						25	850	

Semester-III

Course Code- 106301 Digital Electronics

3 0 0 3

Unit-1.0

7 hrs

Fundamentals of Digital Systems and logic families: Digital signals, digital circuits, AND, OR, NOT, NAND, NOR and Exclusive-OR operations, Boolean algebra, examples of IC gates, number systems-binary, signed binary, octal hexadecimal number, binary arithmetic, one's and two's complements arithmetic, codes, error detecting and correcting codes, characteristics of digital ICs, digital logic families, TTL, Schottky TTL and CMOS logic, interfacing CMOS and TTL, Tri - state logic.

Unit-2.0

7 hrs

Combinational Digital Circuits: Standard representation for logic functions K-map representation, simplification of logic functions using K-map, minimization of logical functions.

Don't care conditions, Multiplexer, DeMultiplexer/Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial adder, ALU, elementary ALU design, popular MSI chips, digital comparator, parity checker/generator, code converters, priority encoders, decoders/drivers for display devices, Q-M method of function realization.

Unit-3.0

7 hrs

Sequential circuits and systems: A 1-bit memory, the circuit properties of Bistable latch, the clocked SR flip flop, J- K-T and D types flip flops, applications of flip flops, shift registers, applications of shift registers, serial to parallel converter, parallel to serial converter, ring counter, sequence generator, ripple (Asynchronous) counters, synchronous counters, counters design using flip flops, special counter IC's, asynchronous sequential counters, applications of counters.

Unit-4.0

7 hrs

A/D and D/A Converters: Digital to analog converters: weighted resistor/converter, R- 2RLadder D/A converter, specifications for D/A converters, examples of D/A converter ICs, sample and hold circuit, analog to digital converters: quantization and encoding, parallel comparator A/D converter, successive approximation A/D converter, counting A/D converter, dual slope A/D converter, A/D converter using

Voltage to frequency and voltage to time conversion, specifications of A/D converters, example of A/D converter ICs.

Unit-5.0

7 hrs

Semiconductor memories: Memory organization and operation, expanding memory size, classification and characteristics of memories, sequential memory, read only memory (ROM), read and write memory(RAM), content addressable memory (CAM), charge de coupled device memory (CCD), commonly used memory chips, ROM as a PLD.

Unit-6.0

7 hrs.

Programmable logic devices

Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).

Text/Reference:

1. R. P. Jain, "Modern Digital Electronics", McGraw Hill Education, 2009.
2. M. M. Mano, "Digital logic and Computer design", Pearson Education India, 2016.
3. A. Kumar, "Fundamentals of Digital Circuits", Prentice Hall India, 2016.



Course Code-106302

Data Structure & Algorithms

3 0 0 3

Unit-1.0**7 hrs**

Introduction: Basic Terminologies: Elementary Data Organizations, Data Structure Operations: insertion, deletion, traversal etc.; Analysis of an Algorithm, Asymptotic Notations, Time-Space trade off.

Unit-2.0**7 hrs**

Stacks and Queues: ADT Stack and its operations: Algorithms and their complexity analysis, Applications of Stacks: Expression Conversion and evaluation – corresponding algorithms and complexity analysis. ADT queue, Types of Queue: Simple Queue, Circular Queue, Priority Queue; Operations on each Type of Queues: Algorithms and their analysis.

Unit-3.0**7 hrs**

Linked Lists: Singly linked lists: Representation in memory, Algorithms of several operations: Traversing, Searching, Insertion into, Deletion from linked list; Linked representation of Stack and Queue, Header nodes, doubly linked list: operations on it and algorithmic analysis; Circular Linked Lists: all operations their algorithms and the complexity analysis.

Unit-4.0**7 hrs**

Searching, Sorting and Hashing: Linear Search and Binary Search Techniques and their complexity analysis. Objective and properties of different sorting algorithms: Selection Sort, Bubble Sort, Insertion Sort, Quick Sort, Merge Sort, Heap Sort; Performance and Comparison among all the methods, Hashing.

Unit-5.0**7 hrs**

Trees: Basic Tree Terminologies, Different types of Trees: Binary Tree, Threaded Binary Tree, Binary Search Tree, AVL Tree; Tree operations on each of the trees and their algorithms with complexity analysis. Applications of Binary Trees. B Tree, B+ Tree: definitions, algorithms and analysis.

Unit-6.0**7 hrs**

Graph: Basic Terminologies and Representations, Graph search and traversal algorithms and complexity analysis.

Text/ Reference:-

1. Algorithms, Data Structures, and Problem Solving with C++”, Illustrated Edition
2. by Mark Allen Weiss, Addison-Wesley Publishing Company.
3. “How to Solve it by Computer”, 2nd Impression by R.G. Dromey, Pearson Education.
4. “Fundamentals of Data Structures”, Illustrated Edition by Ellis Horowitz, Sartaj Sahni, Computer Science Press.

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5. P. J. Deitel, H. M. Deitel, “Java: How to Program”, Prentice Hall, 6th Edition, 2005.
6. P. Radha Krishna, “Object Oriented Programming through Java”, Universities Press, CRC Press, 2007.
7. Bruce Eckel, “Thinking in Java”, Prentice Hall, 4th Edition, 2006.
8. Sachin Malhotra, Saurabh Chaudhary, “Programming in Java”, Oxford University Press, 2nd Edition, 2014.



Course Code- 106304 Discrete Mathematics and Graph Theory 3 1 0 4

Unit-1.0 6 hrs.

Sets, Relation and Function: Operations and Laws of Sets, Cartesian Products, Binary Relation, Partial Ordering Relation, Equivalence Relation, Image of a Set, Sum and Product of Functions, Bijective functions, Inverse and Composite Function, Size of a Set, Finite and infinite Sets, Countable and uncountable Sets, Cantor's diagonal argument and The Power Set theorem, Schroeder-Bernstein theorem.

Unit-2.0 8 hrs.

Principles of Mathematical Induction: The Well-Ordering Principle, Recursive definition, The Division algorithm: Prime Numbers, The Greatest Common Divisor: Euclidean Algorithm, The Fundamental Theorem of Arithmetic.

Basic counting techniques-inclusion and exclusion, pigeon-hole principle, permutation and combination.

Unit-3.0 6 hrs.

Propositional Logic: Syntax, Semantics, Validity and Satisfiability, Basic Connectives and Truth Tables, Logical Equivalence: The Laws of Logic, Logical Implication, Rules of Inference, The use of Quantifiers.

Unit-4.0 4 hrs.

Proof Techniques: Some Terminology, Proof Methods and Strategies, Forward Proof, Proof by Contradiction, Proof by Contraposition, Proof of Necessity and Sufficiency.

Unit-5.0 8 hrs.

Algebraic Structures and Morphism: Algebraic Structures with one Binary Operation, Semi Groups, Monoids, Groups, Congruence Relation and Quotient Structures, Free and Cyclic Monoids and Groups, Permutation Groups, Substructures, Normal Subgroups, Algebraic Structures with two Binary Operation, Rings, Integral Domain and Fields. Boolean Algebra and Boolean Ring, Identities of Boolean Algebra, Duality, Representation of Boolean Function, Disjunctive and Conjunctive Normal Form

Unit-6.0 10 hrs.

Graphs and Trees: Graphs and their properties, Degree, Connectivity, Path, Cycle, Sub Graph, Isomorphism, Eulerian and Hamiltonian Walks, Graph Coloring, Coloring maps and Planar Graphs, Coloring Vertices, Coloring Edges, List Coloring, Perfect Graph, definition properties and Example, rooted trees, trees and sorting, weighted trees and prefix codes, Bi-connected component and Articulation Points, Shortest distances.

Text/Reference:

1. Kenneth H. Rosen, Discrete Mathematics and its Applications, Tata McGraw –Hill
2. Susanna S. Epp, Discrete Mathematics with Applications, 4th edition, Wadsworth Publishing Co.Inc.
3. C L Liu and D P Mohapatra, Elements of Discrete Mathematics A Computer Oriented Approach, 3rd Edition by, Tata McGraw –Hill.
4. J.P. Tremblay and R. Manohar, Discrete Mathematical Structure

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and It's Application to Computer Science",
TMGEdition,TataMcgraw-Hill

5. Norman L. Biggs, Discrete Mathematics, 2nd Edition, Oxford University Press. Schaum's Outlines Series, Seymour Lipschutz, MarcLipson,
6. Discrete Mathematics, Tata McGraw -Hill



Course Code- 106305 Operating Systems **3 0 0 3**

Unit-1.0 **7 hrs.**

Introduction: Concept of Operating Systems, Generations of Operating systems, Types of Operating Systems, OS Services, System Calls, Structure of an OS-Layered, Monolithic, Microkernel Operating Systems, Concept of Virtual Machine. Case study on UNIX and WINDOWS Operating System.

Unit-2.0 **8 hrs.**

Processes: Definition, Process Relationship, Different states of a Process, Process State transitions, Process Control Block (PCB), Context switching.

Thread: Definition, Various states, Benefits of threads, Types of threads, Concept of multithreads

Process Scheduling: Foundation and Scheduling objectives, Types of Schedulers, Scheduling criteria: CPU utilization, Throughput, Turnaround Time, Waiting Time, Response Time; Scheduling algorithms: Pre-emptive and Non pre-emptive, FCFS, SJF, RR; Multiprocessor scheduling: Real Time scheduling: RM and EDF.

Unit-3.0 **8 hrs.**

Inter-process Communication: Critical Section, Race Conditions, Mutual Exclusion, Hardware Solution, Strict Alternation, Peterson's Solution, The Producer - Consumer Problem, Semaphores, Event Counters, Monitors, Message Passing, Shared Memory, Classical IPC Problems: Reader's & Writer Problem, Dining Philosopher Problem etc.

Unit-4.0 **5 hrs.**

Deadlocks: Definition, Necessary and sufficient conditions for Deadlock, Deadlock Prevention, and Deadlock Avoidance: Banker's algorithm, Deadlock detection and Recovery.

Unit-5.0 **7 hrs.**

Memory Management: Basic concept, Logical and Physical address map, Memory allocation: Contiguous Memory allocation – Fixed and variable partition–Internal and External fragmentation and Compaction; Paging and Segmentation: Principle of operation – Page allocation – Hardware support for paging, Protection and sharing, Advantages and Disadvantages of paging and segmentation.

Virtual Memory: Basics of Virtual Memory – Hardware and control structures – Locality of reference, Page fault, Working Set, Dirty page/Dirty bit – Demand paging, Page Replacement algorithms: Optimal, First in First Out (FIFO), Second Chance (SC), Not recently used (NRU) and Least Recently used (LRU).

Unit-6.0 **7 hrs.**

File Management: Concept of File, Access methods, File types, File operation, Directory structure, File System structure, Allocation methods (contiguous, linked, indexed), Free- space management (bit vector, linked list, grouping), directory implementation (linear list, hash table), efficiency and performance.

Disk Management: Disk structure, Disk scheduling - FCFS, SSTF, SCAN, C-SCAN, Disk reliability, Disk formatting, Boot-block, Bad blocks

I/O Hardware: I/O devices, Device controllers, Direct memory access, Principles

of I/O Software: Goals of Interrupt handlers, Device drivers, Device independent I/O software, Secondary-Storage Structure.

Text/Reference:

1. Operating System Concepts Essentials, 9th Edition by Avi Silberschatz, Peter Galvin, Greg Gagne, Wiley Asia Student Edition.
2. Operating Systems: Internals and Design Principles, 5th Edition, William Stallings, Prentice Hall of India.
3. Operating Systems: Design and Implementation 3rd Edition, 3rd Edition, Andrew S. Tanenbaum
4. Modern Operating Systems, 4th Edition, Andrew S. Tanenbaum
5. Operating System: A Design-oriented Approach, 1st Edition by Charles Crowley, Irwin Publishing
Operating Systems: A Modern Perspective, 2nd Edition by Gary J. Nutt, Addison- Wesley
6. Design of the Unix Operating Systems, 8th Edition by Maurice Bach, Prentice-Hall of India
7. Understanding the Linux Kernel, 3rd Edition, Daniel P. Bovet, Marco Cesati, O'Reilly and Associates



Course Code-106306**Universal Human Values****3 0 0 3****Unit- 1.0: Introduction to Value Education****5 hrs**

Right Understanding, Relationship and Physical Facility (Holistic Development and the Role of Education), Understanding Value Education Sharing about Oneself, Self-exploration as the Process for Value Education, Continuous Happiness and Prosperity – the Basic Human Aspirations, Exploring Human Consciousness, Happiness and Prosperity – Current Scenario, Method to Fulfil the Basic Human Aspirations,

Unit- 2.0: Harmony in the Human Being**4 hrs**

Understanding Human being as the Co-existence of the Self and the Body, Distinguishing between the Needs of the Self and the Body, The Body as an Instrument of the Self, Understanding Harmony in the Self, Harmony of the Self with the Body, Programme to ensure self-regulation and Health.

Unit- 3.0: Harmony in the Family and Society**5 hrs**

Harmony in the Family – the Basic Unit of Human Interaction, ‘Trust’ – the Foundational Value in Relationship, ‘Respect’ – as the Right Evaluation, Other Feelings, Justice in Human-to-Human Relationship, Understanding Harmony in the Society, Vision for the Universal Human Order.

Unit- 4.0: Harmony in the Nature/Existence**6 hrs**

Understanding Harmony in the Nature, Interconnectedness, self-regulation and Mutual Fulfilment among the Four Orders of Nature, Realizing Existence as Co-existence at All Levels, The Holistic Perception of Harmony in Existence.

Unit- 5.0: Implications of the Holistic Understanding – a Look at Professional**5 hrs**

Natural Acceptance of Human Values, Definitiveness of (Ethical) Human Conduct, A Basis for Humanistic Education, Humanistic Constitution and Universal Human Order, Competence in Professional Ethics, Holistic Technologies, Production Systems and Management Models-Typical Case Studies, Strategies for Transition towards Value-based Life and Profession .

Unit- 6.0:**3hrs**

Competence in Professional Ethics, Holistic Technologies, Production Systems and Management Models-Typical Case Studies, Strategies for Transition towards Value-based Life and Profession.

Text /Reference:

1. A Foundation Course in Human Values and Professional Ethics, R R Gaur, R Asthana, G P Bagaria, 2nd Revised Edition, Excel Books, New Delhi, 2019. ISBN 978-93-8703447.
2. Jeevan Vidya: Ek Parichaya, A Nagaraj, Jeevan Vidya Prakashan, Amarkantak, 1999.
3. Human Values, A.N. Tripathi, New Age Intl. Publishers, New Delhi, 2004.
4. The Story of Stuff (Book).
5. The Story of My Experiments with Truth – by Mohandas Karamchand Gandhi.
6. Small is Beautiful – E. F Schumacher.
7. Slow is Beautiful – Cecile Andrews.
8. Economy of Permanence – J C Kumarappa.
9. Bharat Mein Angreji Raj – Pandit Sunderlal.
10. Rediscovering India – by Dharampal.
11. Hind Swaraj or Indian Home Rule – by Mohandas K. Gandhi.
12. India Wins Freedom – Maulana Abdul Kalam Azad.
13. Vivekananda – Romain Rolland (English)

Perform any ten Experiments**List of Experiments:**

1. Universal Gates (i) Identification and verification of NAND gate (IC #7400) and NOR gate (IC #7402). (ii) Construction and Verification of all other gate (AND, OR, NOT, XOR) USING a) Only NAND gate b) Only NOR gate
2. Code Convertor & Parity Generator and checker. (i) Identification & verification of NOT (7404), AND (7408) OR (7432) & XOR (7486) gates. (ii) Design, construction and verification of 3-bit Binary to Gray convertor and 3-bit Grey to Binary convertor circuit. (iii) Design, construction and verification of 3-bit odd/even Parity Generator and 4-bit odd/even parity checker circuit.
3. Adder, Subtractor & Magnitude comparator circuits. (i) Design, construction and verification of Half Adder and Half Subtractor circuit. (ii) Design, construction and verification of Full Adder and Full Subtractor circuit. (iii) Design, construction and verification of 1-bit and 4-bit Magnitude comparator. (iv) BCD Adder/Subtractor
4. Decoder, MUX & DMUX (i) Construction and verification of BCD to 7-segment decoder using IC # 7447 (ii) Verification of 4:1 MUX, 8:1 MUX & 16:1 MUX. (iii) Verification of 1:4 DMUX, 1:8 DMUX (iv) Cascading of MUX and Cascading of Decoders.
5. Latches and Flip Flops (i) Construction and Verification of a Latch circuit using NAND/NOR gates. (ii) Construction and Verification of S-R Flip Flop using above Latch circuits. (iii) Verification of J-K Flip Flop using IC # 7476 (Dual J-KFF) (iv) Construction and Verification of D-Flip Flop and T-Flip Flop using J-K FF (IC #7476). (v) Construction and Verification of Master Slave J-K Flip Flop.
6. Shift Registers (i) Verification of D-FF using IC # 7474 (Dual D- FF). (ii) Construction and verification of a 2-bit Shift Right Register using IC # 7474 (iii) Construction and verification of a 2-bit Shift Left Register using IC # 7474 (iv) Verification of SISO, SIPO, PISO & PIPO Shift Registers.
7. Synchronous & Asynchronous Counters (i) Construction and verification of 2-bit Ripple counter using J-K FF. (ii) Construction and verification of Mod-3 up and Mod-3 down synchronous counter. (iii) Construction and verification of 2-bit Ring counter using J-K FF. (iv) Construction and verification of 2-bit twisted Ring (Johnson) counter using J-K FF.
8. Design and construction of a 4 bit sequence generator
9. Digital to Analog Converter (DAC). Construction & Verification of D/A converters using following methods.
 - a) Weighted Resistor type
 - b) R-2R ladder network type
10. Analog to Digital Converter (ADC). Construction & Verification of A/D Converter using following methods.
 - a) Counter type
 - b) Successive Approximation type
11. Familiarization with multisim. Design of various Digital Circuits using Multisim.

Perform any ten Experiments**List of Experiments:**

1. Write a program to read a linear list of items and store it in an array.
2. Write a program to implement binary search.
3. Write a program to implement stack using array.
4. Write a program to implement stack using linked list.
5. Write a program to convert infix expression into postfix expression.
6. Write a program to implement queue using array.
7. Write a program to insert element in a circular queue using array.
8. Write a program to implement queue using Linked List.
9. Implement single linked list:
 - a. Create a single linked list.
 - b. Count number of nodes.
 - c. Traverse the linked list.
10.
 - a. a.Insert node in singly linked list from beginning.
 - b. Insert a node at certain position
11. Delete a node of singly linked list:
 - a. from beginning
 - b. from end
 - c. at certain position
 - d. delete entire list
 - e. Reverse the single linked list
12. Insert a node in the doubly linked list:
 - a. from beginning
 - b. from end
 - c. at a certain position
 - d. Reverse the list
13. Delete a node of doubly linked list:
 - a. from beginning
 - b. from end
 - c. at certain position
14. Create a node of circular singly linked list and circular doubly linked list.
15. Write a program for tree traversal:
 - a. Preorder
 - b. Inorder
 - c. Postorder

Course Code-106303P Object Oriented Programming using JAVA Lab

0 0 2 1

Perform all Experiments

List of programs:

1. Program to Demonstrate Basic Java Syntax and Control Structures
2. Program Using Classes, Objects, Methods, and Constructors
3. Program on Method Overloading and Constructor Overloading
4. Program to Demonstrate Inheritance and Use of 'super' Keyword
5. Program Using Method Overriding and Runtime Polymorphism
6. Program to Implement Abstract Class and Interface
7. Program on User-Defined Exceptions
8. Multithreading Program with Synchronization
9. File Handling Program Using Byte Stream & Character Stream.
10. Program Using Java Collections Framework & JDBC Connectivity.



Perform all Experiments

Operating System Lab: -

1. Write a program to implement FCFS scheduling algorithm.
2. Write a program to implement SJF scheduling algorithm.
3. Write a program to implement priority scheduling algorithm.
4. Write a program to implement round robin scheduling.
5. Write a program to implement banker's algorithm.
6. Write a device driver for any device or peripheral.
7. Write a program to implement disk scheduling algorithm.
8. Write a program to implement dining philosopher problem.
9. Write a program to implement producer consumer problem.
10. Write a program to implement LRU page replacement algorithm.



B. Tech (Information Technology)

(SESSION- 2024-28 onwards)

Course Code-106308

Internship – I

02 Weeks (2 Credits)

Internship I Guidelines:

Internship I is of a minimum duration of two weeks which can be completed in an Industry/Institute in consultation with concerned Engineering College/ Institute. After completion of internship a detailed report of the internship mentioning the training undertaken along with certificate should be submitted.

